MODEL

CONTENTS

MICRO COMPONENT SYSTEM

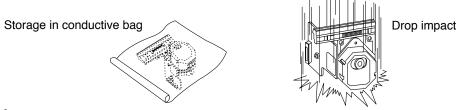
1. SERVICING PRECAUTIONS 3
2. ESD PRECAUTIONS
3. SPECIFICATIONS 6
4. ADJUSTMENTS 8
5. MAJOR WAVEFORM
6. TROUBLESHOOTING GUIDE
7. BLOCK DIAGRAM
8. SCHEMATIC DIAGRAM
• FRONT & KEY CIRCUIT 20
• AMP & DECK CIRCUIT 21
• TUNER CIRCUIT 22
• CDP CIRCUIT
9. WIRING DIAGRAM
10. PCB LAYOUTS 25~26
• MAIN P.C.BOARD
• CDP P.C. BOARD
11. INTERNAL BLOCK DIAGRAM OF ICs 27
12. EXPLODED VIEW/PARTS LIST
• CABINET 38
• TAPE DECK MECHANISM: AUTO STOP DECK
13. REPLACEMENT PARTS LIST 41~52
SPEAKER SYSTEM
1. SPECIFICATION
2. SCHEMATIC DIAGRAM 53
3. EXPLODED VIEW/PARTS LIST 54

SERVICING PRECAUTIONS

NOTES REGARDING HANDLING OF THE PICK-UP

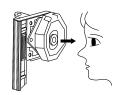
1. Notes for transport and storage

- 1) The pick-up should always be left in its conductive bag until immediately prior to use.
- 2) The pick-up should never be subjected to external pressure or impact.



2. Repair notes

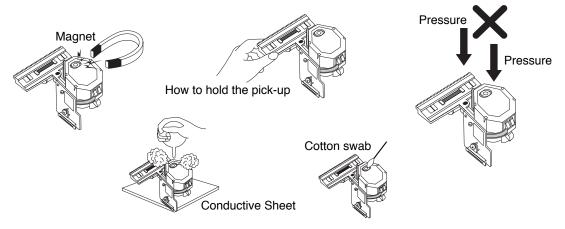
- 1) The pick-up incorporates a strong magnet, and so should never be brought close to magnetic materials.
- 2) The pick-up should always be handled correctly and carefully, taking care to avoid external pressure and impact. If it is subjected to strong pressure or impact, the result may be an operational malfunction and/or damage to the printed-circuit board.
- 3) Each and every pick-up is already individually adjusted to a high degree of precision, and for that reason the adjustment point and installation screws should absolutely never be touched.
- 4) Laser beams may damage the eyes! Absolutely never permit laser beams to enter the eyes! Also NEVER switch ON the power to the laser output part (lens, etc.) of the pick-up if it is damaged.



NEVER look directly at the laser beam, and don't let contact fingers or other exposed skin.

5) Cleaning the lens surface

If there is dust on the lens surface, the dust should be cleaned away by using an air bush (such as used for camera lens). The lens is held by a delicate spring. When cleaning the lens surface, therefore, a cotton swab should be used, taking care not to distort this.



6) Never attempt to disassemble the pick-up.

Spring by excess pressure. If the lens is extremely dirty, apply isopropyl alcohol to the cotton swab. (Do not use any other liquid cleaners, because they will damage the lens.) Take care not to use too much of this alcohol on the swab, and do not allow the alcohol to get inside the pick-up.

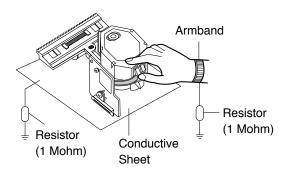
NOTES REGARDING COMPACT DISC PLAYER REPAIRS

1. Preparations

- 1) Compact disc players incorporate a great many ICs as well as the pick-up (laser diode). These components are sensitive to, and easily affected by, static electricity. If such static electricity is high voltage, components can be damaged, and for that reason components should be handled with care.
- 2) The pick-up is composed of many optical components and other high-precision components. Care must be taken, therefore, to avoid repair or storage where the temperature of humidity is high, where strong magnetism is present, or where there is excessive dust.

2. Notes for repair

- 1) Before replacing a component part, first disconnect the power supply lead wire from the unit
- 2) All equipment, measuring instruments and tools must be grounded.
- 3) The workbench should be covered with a conductive sheet and grounded. When removing the laser pick-up from its conductive bag, do not place the pick-up on the bag. (This is because there is the possibility of damage by static electricity.)
- 4) To prevent AC leakage, the metal part of the soldering iron should be grounded.
- 5) Workers should be grounded by an armband $(1M\Omega)$
- 6) Care should be taken not to permit the laser pick-up to come in contact with clothing, in order to prevent static electricity changes in the clothing to escape from the armband.
- 7) The laser beam from the pick-up should NEVER be directly facing the eyes or bare skin.



ESD PRECAUTIONS

Electrostatically Sensitive Devices (ESD)

Some semiconductor (solid state) devices can be damaged easily by static electricity. Such components commonly are called Electrostatically Sensitive Devices (ESD). Examples of typical ESD devices are integrated circuits and some field-effect transistors and semiconductor chip components. The following techniques should be used to help reduce the incidence of component damage caused by static electricity.

- Immediately before handling any semiconductor component or semiconductor-equipped assembly, drain off
 any electrostatic charge on your body by touching a known earth ground. Alternatively, obtain and wear a
 commercially available discharging wrist strap device, which should be removed for potential shock reasons
 prior to applying power to the unit under test.
- 2. After removing an electrical assembly equipped with ESD devices, place the assembly on a conductive surface such as aluminum foil, to prevent electrostatic charge buildup or exposure of the assembly.
- 3. Use only a grounded-tip soldering iron to solder or unsolder ESD devices.
- 4. Use only an anti-static solder removal device. Some solder removal devices not classified as "anti-static" can generate electrical charges sufficient to damage ESD devices.
- 5. Do not use freon-propelled chemicals. These can generate electrical charges sufficient to damage ESD devices.
- 6. Do not remove a replacement ESD device from its protective package until immediately before you are ready to install it. (Most replacement ESD devices are packaged with leads electrically shorted together by conductive foam, aluminum foil or comparable conductive materials).
- 7. Immediately before removing the protective material from the leads of a replacement ESD device, touch the protective material to the chassis or circuit assembly into which the device will by installed.

CAUTION: BE SURE NO POWER IS APPLIED TO THE CHASSIS OR CIRCUIT, AND OBSERVE ALL OTHER SAFETY PRECAUTIONS.

8. Minimize bodily motions when handing unpackaged replacement ESD devices. (Otherwise harmless motion such as the brushing together of your clothes fabric or the lifting of your foot from a carpeted floor can generate static electricity sufficient to damage an ESD device).

[CAUTION. GRAPHIC SYMBOLS]



THE LIGHTNING FLASH WITH APROWHEAD SYMBOL. WITHIN AN EQUILATERAL TRIANGLE, IS INTENDED TO ALERT THE SERVICE PERSONNEL TO THE PRESENCE OF UNINSULATED "DANGEROUS VOLTAGE" THAT MAY BE OF SUFFICIENT MAGNITUDE TO CONSTITUTE A RISK OF ELECTRIC SHOCK.



THE EXCLAMATION POINT WITHIN AN EQUILATERAL TRIANGLE IS INTENDED TO ALERT THE SERVICE PERSONNEL TO THE PRESENCE OF IMPORTANT SAFETY INFORMATION IN SERVICE LITERATURE.

ADJUSTMENTS

This set has been aligned at the factory and normally will not require further adjustment. As a result, it is not recommended that any attempt is made to modificate any circuit. If any parts are replaced or if anyone tampers with the adjustment, realignment may be necessary.

ADJUSTMENT & TEST POINT

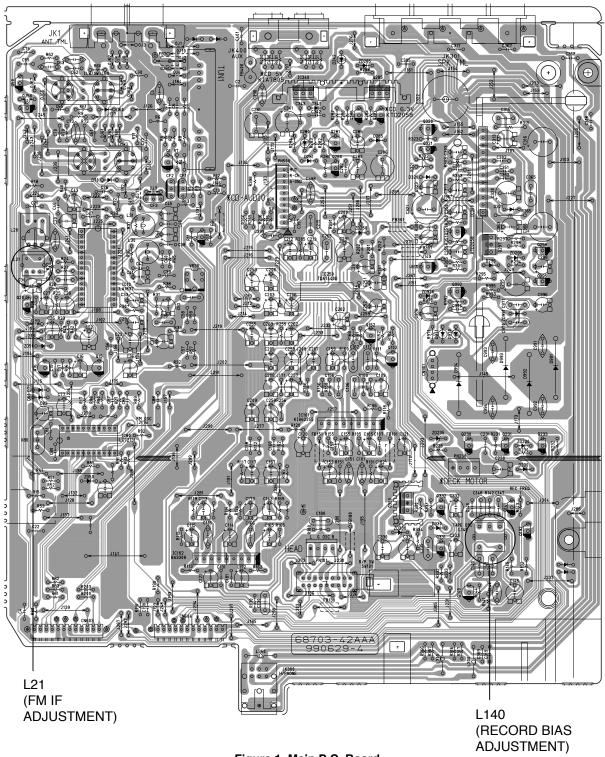


Figure 1. Main P.C. Board

TUNER ADJUSTMENT

Item Test Point		Adjustment	Adjust for
DC Voltage	IC10 26, 28 pin	L21	0V±50mV

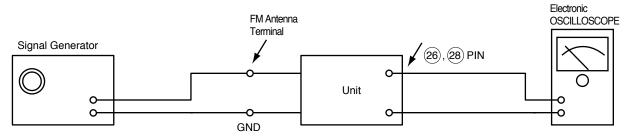


Figure 2. Tuner(S curve) Adjustment Connection Diagram

TAPE DECK ADJUSTMENT

1. AZIMUTH ADJUSTMENT

Deck Mode	Test Tape	Test Point	Adjustment	Adjust for	Remark
Playback	MTT-114	Speaker Terminal	Head Screw	R/L Maximum	Forward:Righthand Side Screw Reverse:Lefthand Side Screw

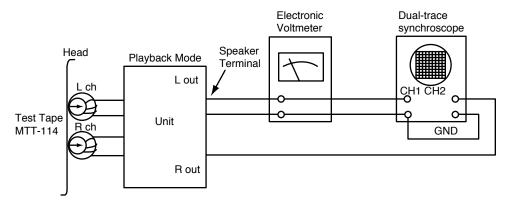


Figure 3. Azimuth Adjustment Connection Diagram

2. RECORD BIAS ADJUSTMENT

Deck Mode	Test Tape	Test Point	Adjustment	Adjust for
Rec/Pause	MTT-5511	Erase Head Wire	L140	83kHz±5kHz

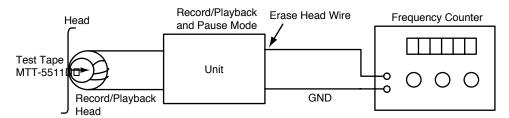


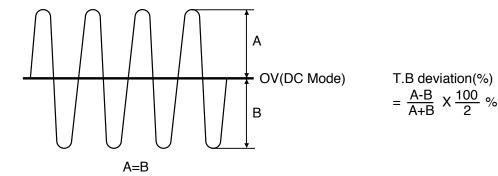
Figure 4. Record Bias Adjustment Connection Diagram

CDP ADJUSTMENTS

· When change the pick-up must be confirm as follow

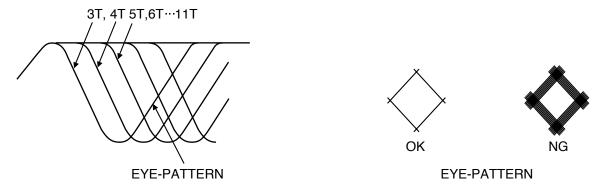
1. TRACKING BALANCE CONFIRMATION

- 1) Connect the oscilloscope to TEO and REF.(IC501 pin 54 and 71)
- 2) Access from 1st selection to last section of test disc (YEDS-18)
- 3) Confirm the normal state of tracking error signal (T.B deviation : less than ±3%)



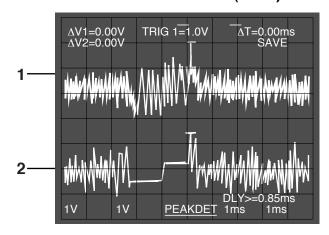
2. RF WAVEFORM CONFIRMATION

- 1) Connect the oscilloscope to RF and REF.(IC501 pin 74 and 71)
- 2) Put a test disc (SONY YEDS-18) into unit and playback the 18th selection of the test disc.
- 3) Confirm the normal state of RF waveform.
- 4) Confirm the less than 30nS of Jitter Meter reading.



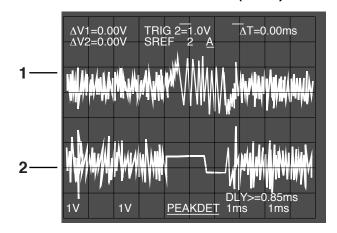
MAJOR WAVEFORM

TRACKING ERROR(REW)



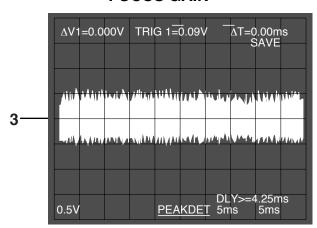
- Connection : 1. IC501 pin (54) (TEO) 2. IC501 pin (50)
- Inspection : Check tracking servo
- circuit.(RWD)

TRACKING ERROR(FWD)



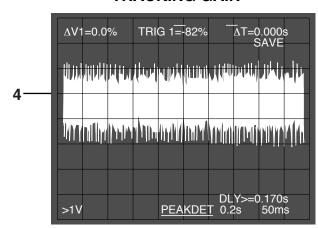
- Connection : 1. IC501 pin (54).(TEO)
 - 2. IC501 pin (50)
- Inspection : Check tracking servo
 - circuit.(RWD)

FOCUS GAIN



- Connection : 3. IC502 pin (1) and (2).
 - Test disc : YEDS-43
- · Inspection : Confirm focus servo circuit.

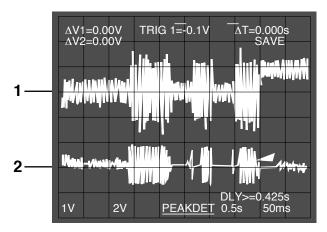
TRACKING GAIN



- Connection : 3. IC502 pin (26) and (27).
 - Test disc: YEDS-43
- Inspection: Confirm TRACK servo circuit.

TRACKING COIL DRIVE

E.F. BALANCE



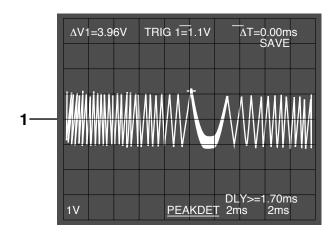


2. IC501 pin (50)

• Inspection : - Confirm tracking servo circuit.

- Check IC501 (Cold solder joint

or short circuit)

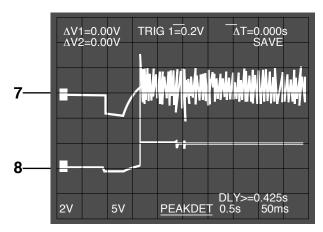


• Connection : 1. IC501 pin (54).

• Inspection : Confirm tacking servo balance

deviation rate

READING

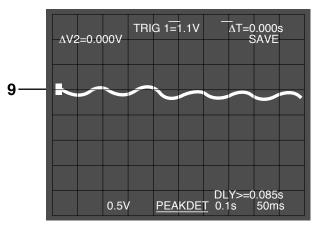


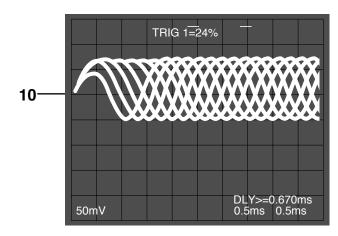
• Connection: 7. IC501 pin 48.

8. IC501 pin (40) (FOK)

• Inspection: Check IC502 pin (4) to IC501 PIN

(48) (Pattern defective)



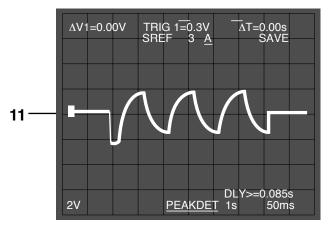


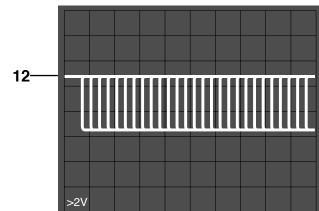
- Connection : 9. IC502 pin (7) and (8)
- Inspection : Check IC501 pin (43) to IC502
 - pin 20 (Pattern defective)
 - Check voltage. (IC502 pin 20)

• Connection : 10. IC501 pin (74).

• Inspection : Check objective Lens of Pickup

clear or not





- Connection : 11. IC502 pin (1) and (2).
- Inspection : Is focus search signal output to

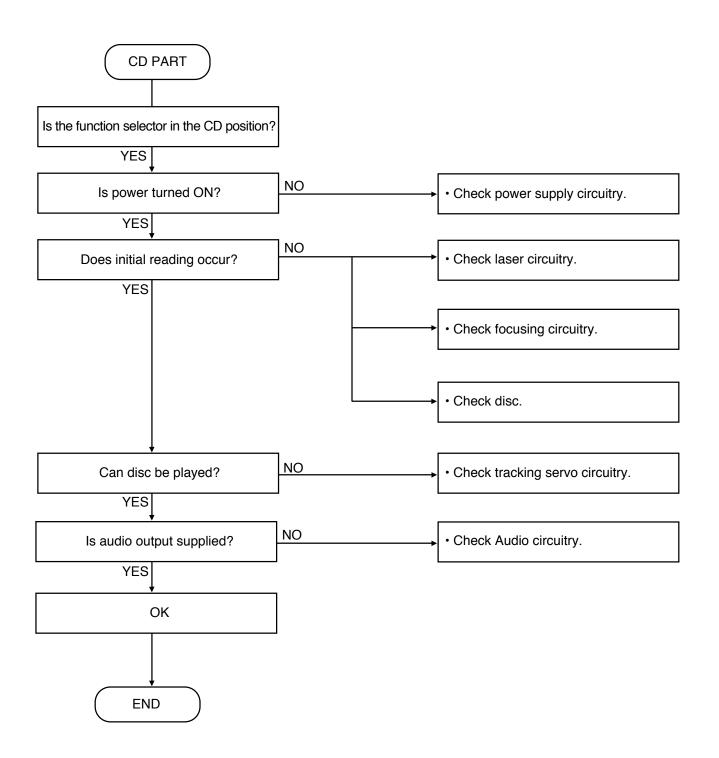
IC501 pin 48?

- Connection : 12. IC501 pin 33.
- Inspection : Check IC503 and surrounding

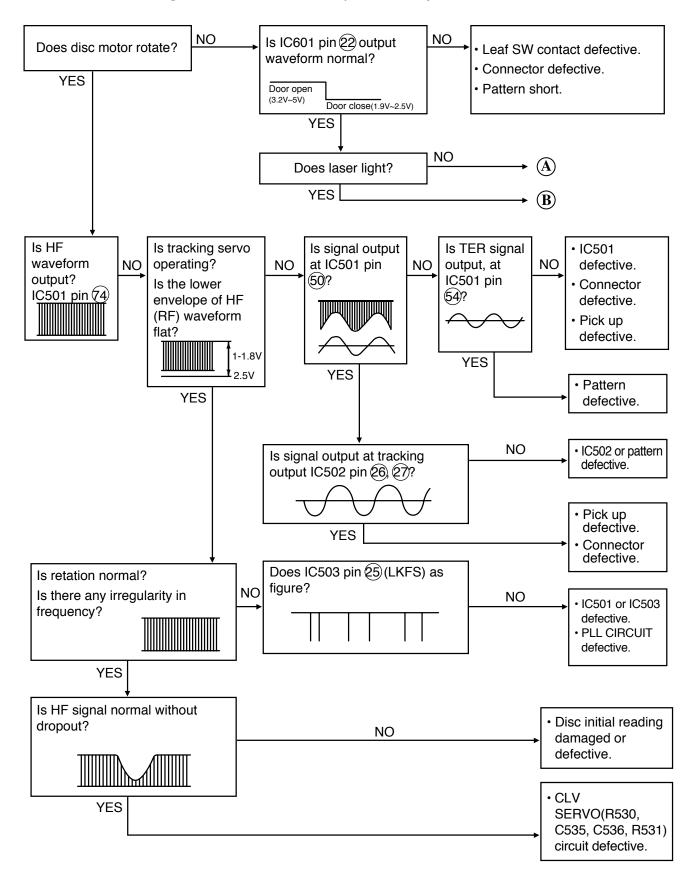
circuit (Cold solder joint or short

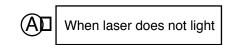
circuit)

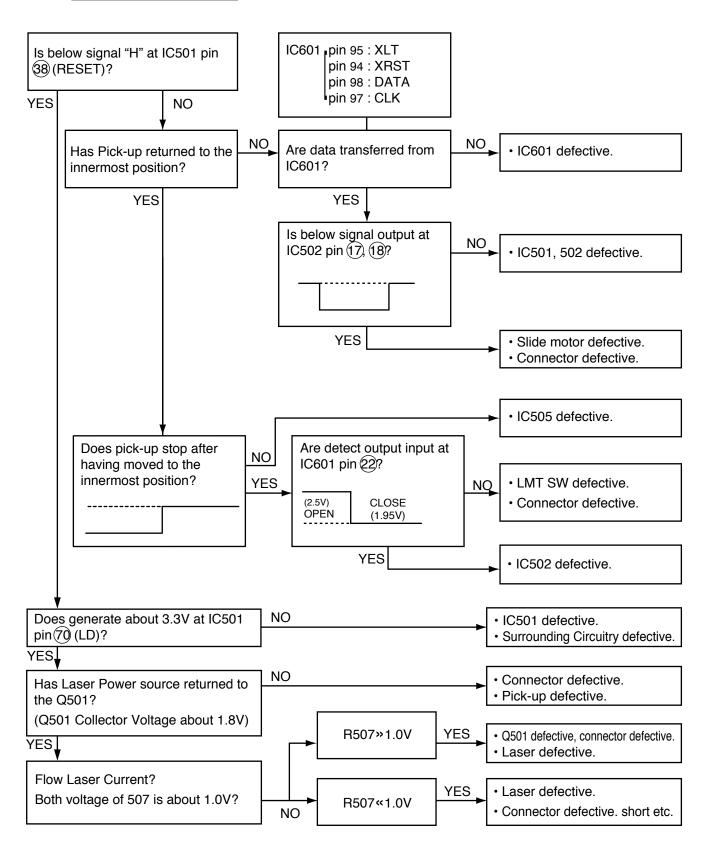
TROUBLESHOOTING GUIDE

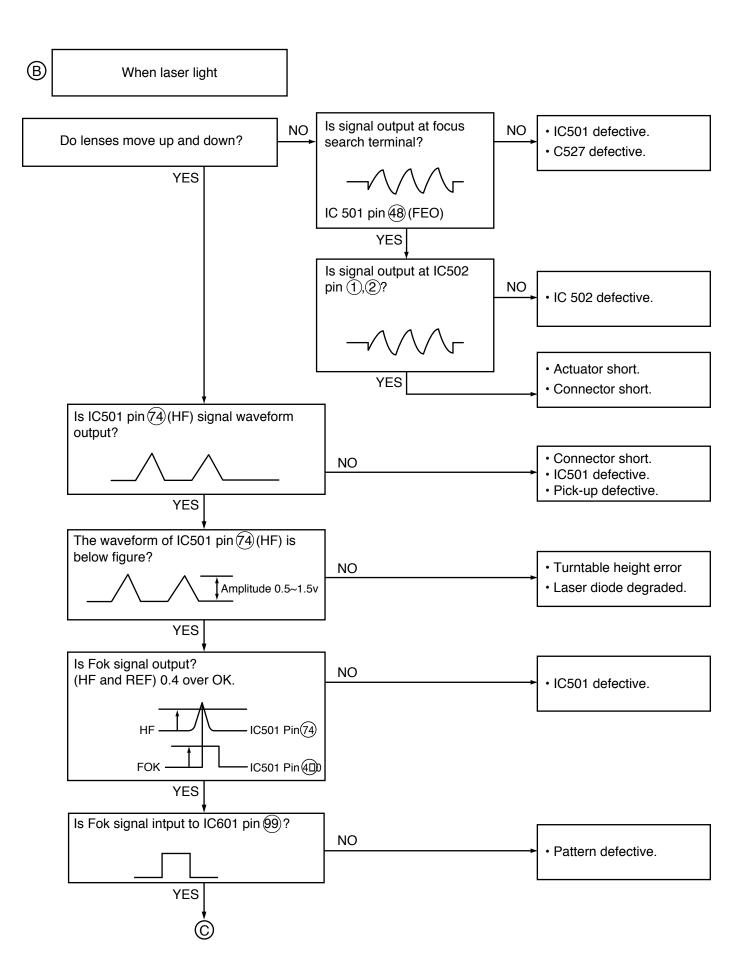


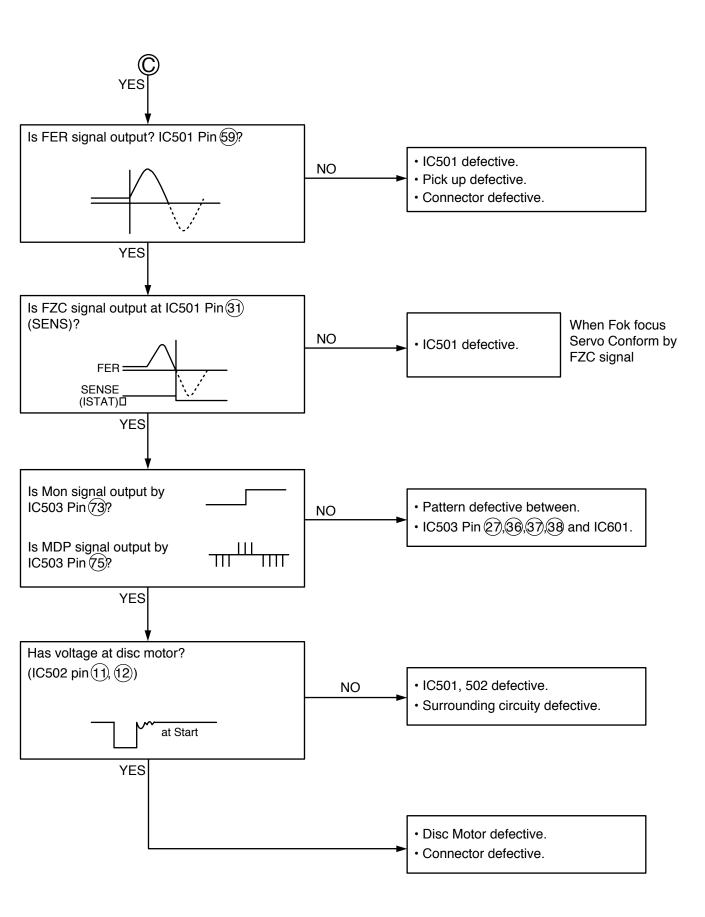
1. If initial reading is not carried out (with disc)



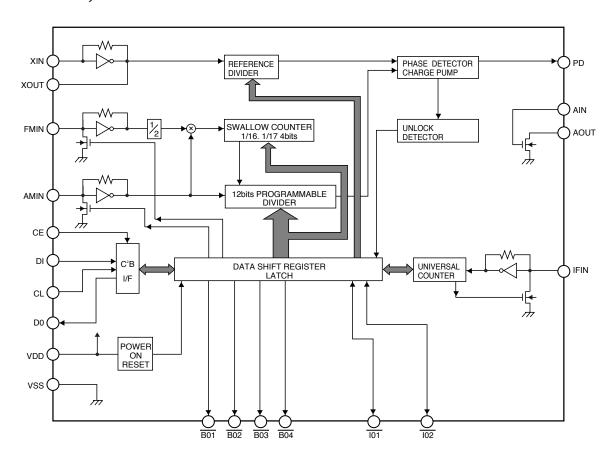




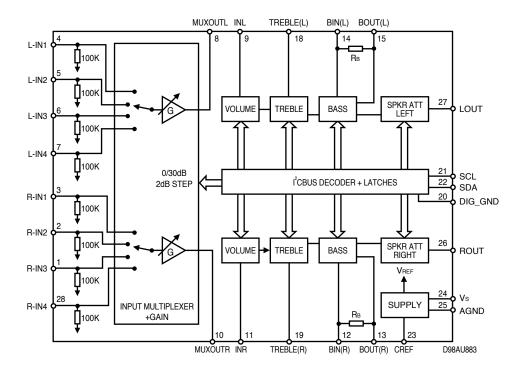




■ LC72131, 72131M



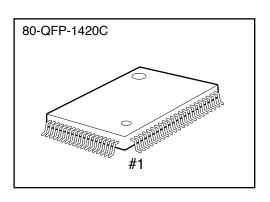
■ TDA7440D



■ KB9223(IC501)

OVERVIEW

The KB9223 is a 1-chip BICMOS intergrated circuit to perform the function of RF AMP and Servo signal processor for compact disc player application. It consist of blocks for RF signal processing, focus, tracking, sled and spindle servo. Also this IC has adjustment free function and embeded opamp for audio post filter.



FEATURES

- · RF amplifier & RF equalizer
- · Focus error amplifier & servo control
- · Tracking error amplifier & servo control
- · Mirror & Defect detector circuit
- Focus OK detrector circuit
- APC(Auto Laser Power Control) circuit for constant laser power
- · FE bias & focus servo offset adjustment free
- EF balance & tracking error gain adjustment free
- · Embeded audio post filter
- The circuit for Interruption countermeasure
- · Double speed play available
- Operating voitage range 3.4V~5.5V

ORDERING INFORMATION

Device	Package	Tempe. Range
KB9223	80-QFP-1420C	-20~+70°C

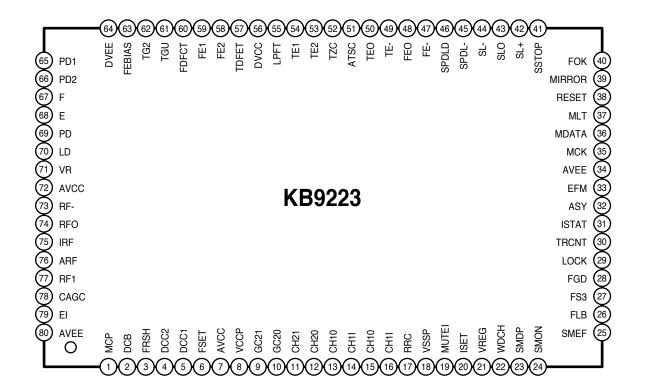
APPLICATIONS

- CD PLAYER
- · Video-CD

RELATED PRODUCT

- KS9286 Data Processor
- KS9284 Data Processor
- KS9258D/KA9259D Motor Driver

PIN CONFIGURATION



PIN DESCRIPTION

1 MCP Capacitor connection pin for mirror hold 2 DCB Capacitor connection pin for defect Bottom hold 3 FRSH Capacitor connection pin for time constant to generate focus search waveform 4 DCC2 The input pin through capacitor of defect bottom hold output 5 DCC1 The output pin of defect bottom hold 6 FSET The peak frequency setting pin for focus, tracking servo and cut off frequency of CLV LPF 7 VDDA Analog ACC for servo part 8 VCCP VCC for post filter 9 GC21 Amplifier output pin for gain and low pass filtering of DAC output CH2 10 GC20 Amplifier output pin for gain and low pass filtering of DAC output CH2 11 CH21 The input pin for post filter channel2 12 CH20 The output pin for post filter channel2 13 CH10 The output pin for post filter channel1 14 CH11 The input pin for post filter channel1 15 GC10 Amplifier output pin for gain and low pass filtering of DAC output CH1 16 GC11 Amplifier negative input pin for gain and low pass filtering of DAC output CH1 17 RRC The pin for noise reduction of post filter bias 18 VSSP VSS for post filter 19 MUTEI The input pin for post filter muting control 10 The input pin for post filter muting control 11 The input pin for current setting of focus search, track jump and sled okick voltage 11 VREG The output pin for rauto sequence 12 SMDP The input pin for spindle servo ON through SMON of DSP 15 SMEF The input pin for spindle servo ON through SMON of DSP 16 Capacitor connection pin to perform rising low bandwidth of focus loop 17 FS3 Capacitor connection pin to perform rising low bandwidth of focus loop 18 Capacitor connection pin to perform rising low bandwidth of focus loop 19 LOCK Sled runaway prevention pin 10 TRCNT Track count output pin 11 Istat Internal status output pin 12 ASY The input pin for asymmetry control 13 EFM EPM comparator output pin 14 VSSA Analog VSS for servo part 15 MCK Micom clock input pin	Pin No.	Symbol	Description
FRSH Capacitor connection pin for time constant to generate focus search waveform DCC2 The input pin through capacitor of defect bottom hold output The output pin of defect bottom hold FSET The peak frequency setting pin for focus, tracking servo and cut off frequency of CLV LPF Analog ACC for servo part VCCP VCC for post filter GC20 Amplifier output pin for gain and low pass filtering of DAC output CH2 The input pin for post filter channel2 CH20 The output pin for post filter channel2 CH20 The output pin for post filter channel2 CH20 The output pin for post filter channel1 The input pin for post filter channel1 CH11 The input pin for post filter channel1 Applifier output pin for post filter channel1 FRC The pin for noise reduction of post filter bias WSSP VSS for post filter MUTEI The input pin for post filter muting control WSSP The input pin for current setting of focus search, track jump and sled okick voltage WDCK The output pin of regulator The clock input pin for suots equence SMDP The input pin for CLV control output pin SMDP of DSP SMCF The input pin of focus on external LPF time constant EAS SMON The input pin for portide for an external LPF time constant EAS SMON The input pin for portide for an external LPF time constant EAS SMON The input pin for portide for an external LPF time constant EAS SMON The input pin for for output pin some portion between FS3 pin SMCF The input pin for output pin some portion between FS3 pin EAS FGD Reducing high freqency gain with capacitor between FS3 pin SMCF The input pin for asymmetry control AND SMC The input pin for asymmetry control SET In input pin for asymmetry control FROM The input pin for asymmetry control FROM The input pin for asymmetry control FROM The input pin for asymmetry control	1	MCP	Capacitor connection pin for mirror hold
4 DCC2 The input pin through capacitor of defect bottom hold 5 DCC1 The output pin of defect bottom hold 6 FSET The peak frequency setting pin for focus, tracking servo and cut off frequency of CLV LPF 7 VDDA Analog ACC for servo part 8 VCCP VCC for post filter 9 GC21 Amplifier negative input pin for gain and low pass filtering of DAC output CH2 10 GC20 Amplifier output pin for post filter channel2 11 CH21 The output pin for post filter channel2 12 CH20 The output pin for post filter channel1 14 CH11 The input pin for post filter channel1 15 GC10 Amplifier output pin for gain and low pass filtering of DAC output CH1 16 GC11 Amplifier negative input pin for gain and low pass filtering of DAC output CH1 17 RRC The pin for noise reduction of post filter bias VSS Por post filter VSS for post filter 18 VSSP VSS for post filter 19 MUTEI The input pin for outrent setting of focus search, track jump and sled okick voltage	2	DCB	Capacitor connection pin for defect Bottom hold
5 DCC1 The output pin of defect bottom hold 6 FSET The peak frequency setting pin for focus, tracking servo and cut off frequency of CLV LPF 7 VDDA Analog ACC for servo part 8 VCCP VCC for post filter 9 GC2I Amplifier negative input pin for gain and low pass filtering of DAC output CH2 10 GC2O Amplifier output pin for gain and low pass filtering of DAC output CH2 11 CH2I The input pin for post filter channel2 12 CH2O The output pin for post filter channel2 13 CH1O The output pin for post filter channel1 14 CH1I The input pin for post filter channel1 15 GC1O Amplifier output pin for gain and low pass filtering of DAC output CH1 16 GC1I Amplifier negative input pin for gain and low pass filtering of DAC output CH1 17 RRC The pin for noise reduction of post filter bias 18 VSSP VSS for post filter 19 MUTEI The input pin for post filter muting control 20 ISET The input pin for current setting of focus search, track jump and sled okick voltage 21 VREG The output pin of regulator 22 WDCK The clock input pin for auto sequence 23 SMDP The input pin for spindle servo ON through SMON of DSP 24 SMON The input pin for povide for an external LPF time constant 26 FLB Capacitor connection pin to perform ising low bandwidth of focus loop 27 FS3 The pin for high freqency gain change of focus loop with internal FS3 switch 28 FGD Reducing high freqency gain with capacitor between FS3 pin 30 TRCNT Track count output pin 31 ISTAT Internal status output pin 32 ASY The input pin for asymmetry control 33 EFM EFM comparator output pin 34 VSSA Analog VSS for servo part	3	FRSH	Capacitor connection pin for time constant to generate focus search waveform
FSET The peak frequency setting pin for focus, tracking servo and cut off frequency of CLV LPF VDDA Analog ACC for servo part VCCP VCC for post filter GC2I Amplifier negative input pin for gain and low pass filtering of DAC output CH2 The input pin for post filter channel2 CH2I The input pin for post filter channel2 CH2O The output pin for post filter channel2 The output pin for post filter channel1 CH1I The input pin for post filter channel1 CH1I The input pin for post filter channel1 CH1I The input pin for post filter channel1 FGC1O Amplifier output pin for gain and low pass filtering of DAC output CH1 FGC1I Amplifier negative input pin for gain and low pass filtering of DAC output CH1 FRC The pin for noise reduction of post filter bias VSSP VSS for post filter MUTEI The input pin for post filter muting control ISET The input pin for post filter muting control VREG The output pin of regulator VREG The output pin of regulator VREG The output pin of regulator WDCK The clock input pin for auto sequence SMDP The input pin of CLV control output pin SMDP of DSP SMON The input pin for spindle servo ON through SMON of DSP The input pin of provide for an external LPF time constant FLB Capacitor connection pin to perform rising low bandwidth of focus loop FSS The pin for high freqency gain change of focus loop with internal FS3 switch Reducing high freqency gain with capacitor between FS3 pin COCK Sled runaway prevention pin TRCNT Track count output pin Track count output pin TRCNT Track count output pin FFM EFM comparator output pin ANALOG SSA Analog VSS for servo part	4	DCC2	The input pin through capacitor of defect bottom hold output
7 VDDA Analog ACC for servo part 8 VCCP VCC for post filter 9 GC2I Amplifier negative input pin for gain and low pass filtering of DAC output CH2 10 GC2O Amplifier output pin for gain and low pass filtering of DAC output CH2 11 CH2I The input pin for post filter channel2 12 CH2O The output pin for post filter channel2 13 CH1O The output pin for post filter channel1 14 CH1I The input pin for post filter channel1 15 GC1O Amplifier output pin for gain and low pass filtering of DAC output CH1 16 GC1I Amplifier negative input pin for gain and low pass filtering of DAC output CH1 17 RRC The pin for noise reduction of post filter bias 18 VSSP VSS for post filter 19 MUTEI The input pin for post filter muting control 20 ISET The input pin for post filter muting control 21 VREG The output pin of regulator 22 WDCK The clock input pin for auto sequence 23 SMDP The input pin of CLV control output pin SMDP of DSP 24 SMON The input pin for spindle servo ON through SMON of DSP 25 SMEF The input pin of provide for an external LPF time constant 26 FLB Capacitor connection pin to perform rising low bandwidth of focus loop 27 FS3 The pin for high freqency gain with capacitor between FS3 pin 28 LOCK Sled runaway prevention pin 30 TRCNT Track count output pin 31 ISTAT Internal status output pin 32 ASY The input pin for asymmetry control 33 EFM EFM comparator output pin 34 VSSA Analog VSS for servo part	5	DCC1	The output pin of defect bottom hold
8 VCCP VCC for post filter 9 GC2I Amplifier negative input pin for gain and low pass filtering of DAC output CH2 10 GC2O Amplifier output pin for gain and low pass filtering of DAC output CH2 11 CH2I The input pin for post filter channel2 12 CH2O The output pin for post filter channel2 13 CH1O The output pin for post filter channel1 14 CH1I The input pin for post filter channel1 15 GC1O Amplifier output pin for gain and low pass filtering of DAC output CH1 16 GC1I Amplifier negative input pin for gain and low pass filtering of DAC output CH1 17 RRC The pin for noise reduction of post filter bias 18 VSSP VSS for post filter 19 MUTEI The input pin for post filter muting control 20 ISET The input pin for current setting of focus search, track jump and sled okick voltage 21 VREG The output pin of regulator 22 WDCK The clock input pin for auto sequence 23 SMDP The input pin of CLV control output pin SMDP of DSP 24 SMON The input pin of provide for an external LPF time constant 26 FLB Capacitor connection pin to perform rising low bandwidth of focus loop 27 FS3 The pin for high freqency gain change of focus loop with internal FS3 switch 28 FGD Reducing high freqency gain with capacitor between FS3 pin 29 LOCK Sled runaway prevention pin 30 TRCNT Track count output pin 31 ISTAT Internal status output pin 32 ASY The input pin for asymmetry control 33 EFM EFM comparator output pin 34 VSSA Analog VSS for servo part	6	FSET	The peak frequency setting pin for focus, tracking servo and cut off frequency of CLV LPF
9 GC2I Amplifier negative input pin for gain and low pass filtering of DAC output CH2 10 GC2O Amplifier output pin for gain and low pass filtering of DAC output CH2 11 CH2I The input pin for post filter channel2 12 CH2O The output pin for post filter channel2 13 CH1O The output pin for post filter channel1 14 CH1I The input pin for post filter channel1 15 GC1O Amplifier output pin for gain and low pass filtering of DAC output CH1 16 GC1I Amplifier negative input pin for gain and low pass filtering of DAC output CH1 17 RRC The pin for noise reduction of post filter bias 18 VSSP VSS for post filter 19 MUTEI The input pin for post filter muting control 20 ISET The input pin for current setting of focus search, track jump and sled okick voltage 21 VREG The output pin of regulator 22 WDCK The clock input pin for auto sequence 23 SMDP The input pin of CLV control output pin SMDP of DSP 24 SMON The input pin for spindle servo ON through SMON of DSP 25 SMEF The input pin of provide for an external LPF time constant 26 FLB Capacitor connection pin to perform rising low bandwidth of focus loop 27 FS3 The pin for high freqency gain with capacitor between FS3 pin 29 LOCK Sled runaway prevention pin 30 TRCNT Track count output pin 31 ISTAT Internal status output pin 32 ASY The input pin for asymmetry control 33 EFM EFM comparator output pin 34 VSSA Analog VSS for servo part	7	VDDA	Analog ACC for servo part
10 GC2O Amplifier output pin for gain and low pass filtering of DAC output CH2 11 CH2I The input pin for post filter channel2 12 CH2O The output pin for post filter channel2 13 CH1O The output pin for post filter channel1 14 CH1I The input pin for post filter channel1 15 GC1O Amplifier output pin for gain and low pass filtering of DAC output CH1 16 GC1I Amplifier negative input pin for gain and low pass filtering of DAC output CH1 17 RRC The pin for noise reduction of post filter bias 18 VSSP VSS for post filter 19 MUTEI The input pin for post filter muting control 20 ISET The input pin for current setting of focus search, track jump and sled okick voltage 21 VREG The output pin of regulator 22 WDCK The clock input pin for auto sequence 23 SMDP The input pin of CLV control output pin SMDP of DSP 24 SMON The input pin for spindle servo ON through SMON of DSP 25 SMEF The input pin of provide for an external LPF time constant 26 FLB Capacitor connection pin to perform rising low bandwidth of focus loop 27 FS3 The pin for high freqency gain with capacitor between FS3 pin 29 LOCK Sled runaway prevention pin 30 TRCNT Track count output pin 31 ISTAT Internal status output pin 32 ASY The input pin for asymmetry control 33 EFM EFM comparator output pin 34 VSSA Analog VSS for servo part	8	VCCP	VCC for post filter
11 CH2I The input pin for post filter channel2 12 CH2O The output pin for post filter channel2 13 CH1O The output pin for post filter channel1 14 CH1I The input pin for post filter channel1 15 GC1O Amplifier output pin for gain and low pass filtering of DAC output CH1 16 GC1I Amplifier negative input pin for gain and low pass filtering of DAC output CH1 17 RRC The pin for noise reduction of post filter bias 18 VSSP VSS for post filter 19 MUTEI The input pin for post filter muting control 20 ISET The input pin for current setting of focus search, track jump and sled okick voltage 21 VREG The output pin of regulator 22 WDCK The clock input pin for auto sequence 23 SMDP The input pin of CLV control output pin SMDP of DSP 24 SMON The input pin for spindle servo ON through SMON of DSP 25 SMEF The input pin of provide for an external LPF time constant 26 FLB Capacitor connection pin to perform rising low bandwidth of focus loop 27 FS3 The pin for high freqency gain change of focus loop with internal FS3 switch 28 FGD Reducing high freqency gain change of focus loop with internal FS3 switch 29 LOCK Sled runaway prevention pin 30 TRCNT Track count output pin 31 ISTAT Internal status output pin 32 ASY The input pin for asymmetry control 33 EFM EFM comparator output pin 34 VSSA Analog VSS for servo part	9	GC2I	Amplifier negative input pin for gain and low pass filtering of DAC output CH2
The output pin for post filter channel2 CH10 The output pin for post filter channel1 CH11 The input pin for post filter channel1 GC10 Amplifier output pin for gain and low pass filtering of DAC output CH1 GC11 Amplifier negative input pin for gain and low pass filtering of DAC output CH1 RRC The pin for noise reduction of post filter bias VSSP VSS for post filter MUTEI The input pin for post filter muting control ISET The input pin for current setting of focus search, track jump and sled okick voltage VREG The output pin of regulator VREG The cottout pin of regulator WDCK The clock input pin for auto sequence SMDP The input pin for Spindle servo ON through SMON of DSP SMEF The input pin of provide for an external LPF time constant ELB Capacitor connection pin to perform rising low bandwidth of focus loop FS3 The pin for high freqency gain change of focus loop with internal FS3 switch Reducing high freqency gain with capacitor between FS3 pin LOCK Sled runaway prevention pin TRCNT Track count output pin STACT Internal status output pin SFM EFM comparator output pin EFM EFM comparator output pin ANY SSA Analog VSS for servo part	10	GC2O	Amplifier output pin for gain and low pass filtering of DAC output CH2
The output pin for post filter channel1 CH1I The input pin for post filter channel1 GC10 Amplifier output pin for gain and low pass filtering of DAC output CH1 Amplifier negative input pin for gain and low pass filtering of DAC output CH1 The pin for noise reduction of post filter bias VSSP VSS for post filter MUTEI The input pin for post filter muting control ISET The input pin for current setting of focus search, track jump and sled okick voltage VREG The output pin of regulator WDCK The clock input pin for auto sequence SMDP The input pin of CLV control output pin SMDP of DSP MON The input pin for spindle servo ON through SMON of DSP SMEF The input pin of provide for an external LPF time constant Capacitor connection pin to perform rising low bandwidth of focus loop FLB Capacitor connection pin to perform rising low bandwidth of focus loop FGD Reducing high freqency gain change of focus loop with internal FS3 switch Reducing high freqency gain with capacitor between FS3 pin LOCK Sled runaway prevention pin Track count output pin Track count output pin STAT Internal status output pin STAT Internal status output pin EFM comparator output pin EFM comparator output pin	11	CH2I	The input pin for post filter channel2
14 CH1I The input pin for post filter channel1 15 GC1O Amplifier output pin for gain and low pass filtering of DAC output CH1 16 GC1I Amplifier negative input pin for gain and low pass filtering of DAC output CH1 17 RRC The pin for noise reduction of post filter bias 18 VSSP VSS for post filter 19 MUTEI The input pin for post filter muting control 20 ISET The input pin for current setting of focus search, track jump and sled okick voltage 21 VREG The output pin of regulator 22 WDCK The clock input pin for auto sequence 23 SMDP The input pin of CLV control output pin SMDP of DSP 24 SMON The input pin for spindle servo ON through SMON of DSP 25 SMEF The input pin of provide for an external LPF time constant 26 FLB Capacitor connection pin to perform rising low bandwidth of focus loop 27 FS3 The pin for high freqency gain change of focus loop with internal FS3 switch 28 FGD Reducing high freqency gain with capacitor between FS3 pin 29 LOCK Sled runaway prevention pin 30 TRCNT Track count output pin 31 ISTAT Internal status output pin 32 ASY The input pin for asymmetry control 33 EFM EFM comparator output pin 34 VSSA Analog VSS for servo part	12	CH2O	The output pin for post filter channel2
Amplifier output pin for gain and low pass filtering of DAC output CH1 GC11 Amplifier negative input pin for gain and low pass filtering of DAC output CH1 The pin for noise reduction of post filter bias VSSP VSS for post filter MUTEI The input pin for post filter muting control ISET The input pin for current setting of focus search, track jump and sled okick voltage VREG The output pin of regulator VREG The input pin for auto sequence SMDP The input pin of CLV control output pin SMDP of DSP SMON The input pin for spindle servo ON through SMON of DSP SMEF The input pin of provide for an external LPF time constant Capacitor connection pin to perform rising low bandwidth of focus loop FS3 The pin for high freqency gain change of focus loop with internal FS3 switch Reducing high freqency gain with capacitor between FS3 pin LOCK Sled runaway prevention pin Track count output pin Track count output pin Track count output pin SFAT Internal status output pin SFM EFM comparator output pin ASY The input pin for asymmetry control EFM Comparator output pin ANA Analog VSS for servo part	13	CH1O	The output pin for post filter channel1
16 GC1I Amplifier negative input pin for gain and low pass filtering of DAC output CH1 17 RRC The pin for noise reduction of post filter bias 18 VSSP VSS for post filter 19 MUTEI The input pin for post filter muting control 20 ISET The input pin for current setting of focus search, track jump and sled okick voltage 21 VREG The output pin of regulator 22 WDCK The clock input pin for auto sequence 23 SMDP The input pin of CLV control output pin SMDP of DSP 24 SMON The input pin for spindle servo ON through SMON of DSP 25 SMEF The input pin of provide for an external LPF time constant 26 FLB Capacitor connection pin to perform rising low bandwidth of focus loop 27 FS3 The pin for high freqency gain change of focus loop with internal FS3 switch 28 FGD Reducing high freqency gain with capacitor between FS3 pin 29 LOCK Sled runaway prevention pin 30 TRCNT Track count output pin 31 ISTAT Internal status output pin 32 ASY The input pin for asymmetry control 33 EFM EFM comparator output pin 34 VSSA Analog VSS for servo part	14	CH1I	The input pin for post filter channel1
17 RRC The pin for noise reduction of post filter bias 18 VSSP VSS for post filter 19 MUTEI The input pin for post filter muting control 20 ISET The input pin for current setting of focus search, track jump and sled okick voltage 21 VREG The output pin of regulator 22 WDCK The clock input pin for auto sequence 23 SMDP The input pin of CLV control output pin SMDP of DSP 24 SMON The input pin for spindle servo ON through SMON of DSP 25 SMEF The input pin of provide for an external LPF time constant 26 FLB Capacitor connection pin to perform rising low bandwidth of focus loop 27 FS3 The pin for high freqency gain change of focus loop with internal FS3 switch 28 FGD Reducing high freqency gain with capacitor between FS3 pin 29 LOCK Sled runaway prevention pin 30 TRCNT Track count output pin 31 ISTAT Internal status output pin 32 ASY The input pin for asymmetry control 33 EFM EFM comparator output pin 34 VSSA Analog VSS for servo part	15	GC1O	Amplifier output pin for gain and low pass filtering of DAC output CH1
18 VSSP VSS for post filter 19 MUTEI The input pin for post filter muting control 20 ISET The input pin for current setting of focus search, track jump and sled okick voltage 21 VREG The output pin of regulator 22 WDCK The clock input pin for auto sequence 23 SMDP The input pin of CLV control output pin SMDP of DSP 24 SMON The input pin for spindle servo ON through SMON of DSP 25 SMEF The input pin of provide for an external LPF time constant 26 FLB Capacitor connection pin to perform rising low bandwidth of focus loop 27 FS3 The pin for high freqency gain change of focus loop with internal FS3 switch 28 FGD Reducing high freqency gain with capacitor between FS3 pin 29 LOCK Sled runaway prevention pin 30 TRCNT Track count output pin 31 ISTAT Internal status output pin 32 ASY The input pin for asymmetry control 33 EFM EFM comparator output pin	16	GC1I	Amplifier negative input pin for gain and low pass filtering of DAC output CH1
19 MUTEI The input pin for post filter muting control 20 ISET The input pin for current setting of focus search, track jump and sled okick voltage 21 VREG The output pin of regulator 22 WDCK The clock input pin for auto sequence 23 SMDP The input pin of CLV control output pin SMDP of DSP 24 SMON The input pin for spindle servo ON through SMON of DSP 25 SMEF The input pin of provide for an external LPF time constant 26 FLB Capacitor connection pin to perform rising low bandwidth of focus loop 27 FS3 The pin for high freqency gain change of focus loop with internal FS3 switch 28 FGD Reducing high freqency gain with capacitor between FS3 pin 29 LOCK Sled runaway prevention pin 30 TRCNT Track count output pin 31 ISTAT Internal status output pin 32 ASY The input pin for asymmetry control 33 EFM EFM comparator output pin	17	RRC	The pin for noise reduction of post filter bias
ISET The input pin for current setting of focus search, track jump and sled okick voltage VREG The output pin of regulator WDCK The clock input pin for auto sequence SMDP The input pin of CLV control output pin SMDP of DSP SMER The input pin for spindle servo ON through SMON of DSP SMEF The input pin of provide for an external LPF time constant Capacitor connection pin to perform rising low bandwidth of focus loop The pin for high freqency gain change of focus loop with internal FS3 switch Reducing high freqency gain with capacitor between FS3 pin CHARLES SIED Reducing high freqency gain with capacitor between FS3 pin TRCNT Track count output pin TRCNT Track count output pin TRCNT Track count output pin ASY The input pin for asymmetry control ASY The input pin for asymmetry control EFM comparator output pin AND VSSA Analog VSS for servo part	18	VSSP	VSS for post filter
21 VREG The output pin of regulator 22 WDCK The clock input pin for auto sequence 23 SMDP The input pin of CLV control output pin SMDP of DSP 24 SMON The input pin for spindle servo ON through SMON of DSP 25 SMEF The input pin of provide for an external LPF time constant 26 FLB Capacitor connection pin to perform rising low bandwidth of focus loop 27 FS3 The pin for high freqency gain change of focus loop with internal FS3 switch 28 FGD Reducing high freqency gain with capacitor between FS3 pin 29 LOCK Sled runaway prevention pin 30 TRCNT Track count output pin 31 ISTAT Internal status output pin 32 ASY The input pin for asymmetry control 33 EFM EFM comparator output pin 34 VSSA Analog VSS for servo part	19	MUTEI	The input pin for post filter muting control
22 WDCK The clock input pin for auto sequence 23 SMDP The input pin of CLV control output pin SMDP of DSP 24 SMON The input pin for spindle servo ON through SMON of DSP 25 SMEF The input pin of provide for an external LPF time constant 26 FLB Capacitor connection pin to perform rising low bandwidth of focus loop 27 FS3 The pin for high freqency gain change of focus loop with internal FS3 switch 28 FGD Reducing high freqency gain with capacitor between FS3 pin 29 LOCK Sled runaway prevention pin 30 TRCNT Track count output pin 31 ISTAT Internal status output pin 32 ASY The input pin for asymmetry control 33 EFM EFM comparator output pin 34 VSSA Analog VSS for servo part	20	ISET	The input pin for current setting of focus search, track jump and sled okick voltage
SMDP The input pin of CLV control output pin SMDP of DSP SMON The input pin for spindle servo ON through SMON of DSP SMEF The input pin of provide for an external LPF time constant Capacitor connection pin to perform rising low bandwidth of focus loop The pin for high frequency gain change of focus loop with internal FS3 switch Reducing high frequency gain with capacitor between FS3 pin LOCK Sled runaway prevention pin Track count output pin ISTAT Internal status output pin SEM EFM comparator output pin EFM comparator output pin AND VSSA Analog VSS for servo part	21	VREG	The output pin of regulator
SMON The input pin for spindle servo ON through SMON of DSP SMEF The input pin of provide for an external LPF time constant Capacitor connection pin to perform rising low bandwidth of focus loop The pin for high freqency gain change of focus loop with internal FS3 switch Reducing high freqency gain with capacitor between FS3 pin LOCK Sled runaway prevention pin Track count output pin ISTAT Internal status output pin ASY The input pin for asymmetry control EFM comparator output pin KSSA Analog VSS for servo part	22	WDCK	The clock input pin for auto sequence
SMEF The input pin of provide for an external LPF time constant Capacitor connection pin to perform rising low bandwidth of focus loop The pin for high frequency gain change of focus loop with internal FS3 switch Reducing high frequency gain with capacitor between FS3 pin LOCK Sled runaway prevention pin TRCNT Track count output pin ISTAT Internal status output pin ASY The input pin for asymmetry control EFM comparator output pin FM VSSA Analog VSS for servo part	23	SMDP	The input pin of CLV control output pin SMDP of DSP
FLB Capacitor connection pin to perform rising low bandwidth of focus loop FS3 The pin for high frequency gain change of focus loop with internal FS3 switch Reducing high frequency gain with capacitor between FS3 pin LOCK Sled runaway prevention pin TRCNT Track count output pin ISTAT Internal status output pin ASY The input pin for asymmetry control FM Comparator output pin Analog VSS for servo part	24	SMON	The input pin for spindle servo ON through SMON of DSP
FS3 The pin for high frequency gain change of focus loop with internal FS3 switch Reducing high frequency gain with capacitor between FS3 pin LOCK Sled runaway prevention pin TRCNT Track count output pin ISTAT Internal status output pin ASY The input pin for asymmetry control FFM comparator output pin FFM comparator output pin AND Analog VSS for servo part	25	SMEF	The input pin of provide for an external LPF time constant
28 FGD Reducing high frequency gain with capacitor between FS3 pin 29 LOCK Sled runaway prevention pin 30 TRCNT Track count output pin 31 ISTAT Internal status output pin 32 ASY The input pin for asymmetry control 33 EFM EFM comparator output pin 34 VSSA Analog VSS for servo part	26	FLB	Capacitor connection pin to perform rising low bandwidth of focus loop
29 LOCK Sled runaway prevention pin 30 TRCNT Track count output pin 31 ISTAT Internal status output pin 32 ASY The input pin for asymmetry control 33 EFM EFM comparator output pin 34 VSSA Analog VSS for servo part	27	FS3	The pin for high freqency gain change of focus loop with internal FS3 switch
30 TRCNT Track count output pin 31 ISTAT Internal status output pin 32 ASY The input pin for asymmetry control 33 EFM EFM comparator output pin 34 VSSA Analog VSS for servo part	28	FGD	Reducing high freqency gain with capacitor between FS3 pin
31 ISTAT Internal status output pin 32 ASY The input pin for asymmetry control 33 EFM EFM comparator output pin 34 VSSA Analog VSS for servo part	29	LOCK	Sled runaway prevention pin
32 ASY The input pin for asymmetry control 33 EFM EFM comparator output pin 34 VSSA Analog VSS for servo part	30	TRCNT	Track count output pin
33 EFM EFM comparator output pin 34 VSSA Analog VSS for servo part	31	ISTAT	Internal status output pin
34 VSSA Analog VSS for servo part	32	ASY	The input pin for asymmetry control
	33	EFM	EFM comparator output pin
35 MCK Micom clock input pin	34	VSSA	Analog VSS for servo part
	35	MCK	Micom clock input pin

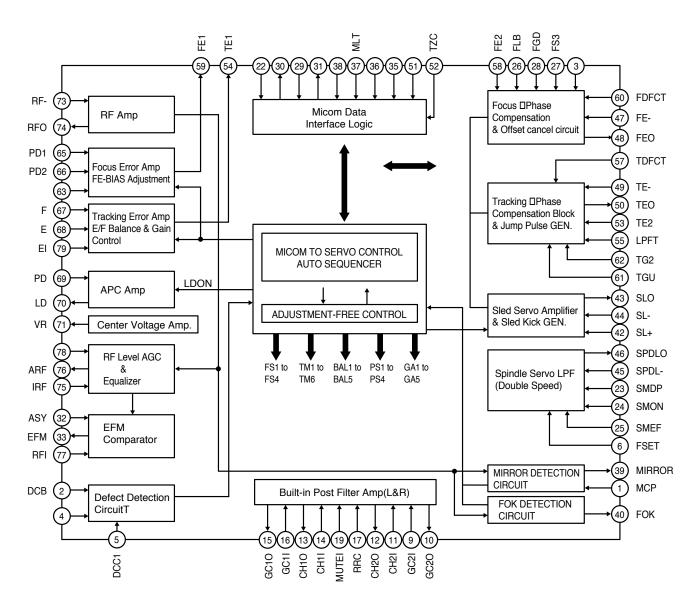
PIN DESCRIPTION (Continued)

Pin No.	Symbol	Description
36	MDATA	Micom data input pin
37	MLT	Micom data latch input pin
38	RESET	Reset input pin
39	MIRROR	The mirror output for test
40	FOK	The output pin of focus OK comparator
41	SSTOP	The pin for detection whether pick_up position is innermost or ton
42	SL+	The noninverting input pin of sled servo amplifier
43	SLO	The output pin of sled servo amplifier
44	SL-	The inverting input pin of sled servo amplifier
45	SPDL-	The noninverting input pin of spindle servo amplifier
46	SPDLO	The output pin of spindle servo amplifier
47	FE-	The inverting input pin of focus servo amplifier
48	FEO	The output pin of focus servo amplifier
49	TE-	The inverting input pin of tracking servo amplifier
50	TEO	The output pin of tracking servo amplifier
51	ATSC	The input pin for Anti-shock detection
52	TZC	The comaparator input pin for tracking zero crossing detection
53	TE2	Tracking servo input pin
54	TE1	Tracking error amplifier output pin
55	LPFT	The input pin of tracking error low pass filtering signal
56	DVDD	The power supply pin for logic circuit
57	TDFCT	The capacitor connection pin for tracking defect compensation
58	FE2	Focus servo input pin
59	FE1	Focus error amplifier output pin
60	FDFCT	The capacitor connection pin for focus defect compensation
61	TGU	The capacitor connection pin for high frequency tracking gain switch
62	TG2	The pin for high frequency gain change of tracking servo loop with internal TG2 switch
63	FEBIAS	Focus error bias voltage control pin
64	DVEE	The DVEE pin for logic circuit
65	PD1	The negative input pin of RF I/V amplifier1 (A+C signal)
66	PD2	The negative input pin of RF I/V amplifier2 (B+D signal)
67	F	The negative input pin of F I/V amplifier1 (F signal
68	Е	The negative input pin of E I/V amplifier1 (E signal)
69	PD	The input pin for APC
70	LD	The output pin for APC

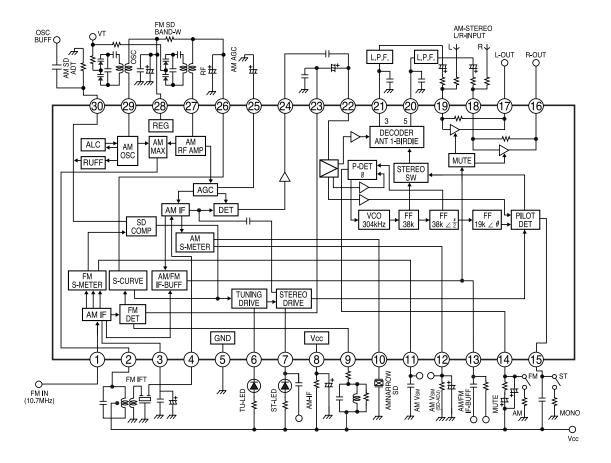
PIN DESCRIPTION (Continued)

Pin No.	Symbol	Description
71	VR	The output pin of (AVEE+AVCC)/2 voltage
72	VCC	VCC for RF part
73	RF-	RF summing amplifier inverting input pin
74	RFO	RF summing amplifier output pin
75	IRF	The input pin for AGC
76	ARF	The output pin for AGC
77	RFI	The input pin for EFM comparating
78	CAGC	The capacitor connection pin for AGC
79	El	Feedback input pin of E I/V amplifier for EF Balance control
80	GND	GND for part

BLOCK DIAGRAM



■ LA1837



■ KB9286

DIGITAL SIGNAL PROCESSOR

The KS9286 is a CMOS integrated circuit designed for the Digital Audio Signal Processor for Compact Disc Player. It is a monolithic IC that builts-in 16 bit Digital Analog Convertor, ESP interface and Digital De-emphasis additional conventional DSP function.

80-QFP-1420C #1

FEATURES

- · EFM data demodulation
- Frame sync datection/protection/insertion
- Powerful error correction (C1 : 2error, C2 : 4erasure)
- Interpolation
- 8fs digital filter (51th+13th+9th)
- · Subcode data serial output
- · CLV servo controller
- Micom interface
- Digital audio output
- Digital addio output
- Digital de-emphasis
- ESP interface
- Built-in 16K SRAM
- Built-in Digital PLL
- · Double speed play available
- · Built-in 16 bit D/A converter
- VDD = $3.4 \sim 5.5$ V

ORDERING INFORMATION

Device	Package	Tempe. Range
KB9286	80-QFP-1420C	-20~+75°C

PIN CONFIGURATION



PIN DESCRIPTION

PIN NO	SYMBOL	10	DESCRIPTION
1	AVDD1	-	Analog VCC1
2	DPDO	0	Charge pump output for Digital PLL
3	DPFIN	ı	Filter input for Digital PLL
4	DPFOUT	0	Filter output for Digital PLL
5	CNTVOL	I	VCO control voltage for Digital PLL
6	AVSS1	-	Analog Ground1
7	DATX	0	Digital Audio output data
8	XIN	I	X'tal oscillator input
9	XOUT	0	X'tal oscillator output
10	WDCHO	0	Word clock output of 48 bit/Slot (88.2KHz)
11	LRCHO	0	Channel clock output of 48 bit/Slot (44.1KHz), 88.2KHz when ESP ON
12	ADATAO	0	Serial audio data output of 48 bit/Slot(MSB first), double speed output when ESP ON
13	DVSS1	-	Digital Ground1
14	ВСКО	0	Audio data bit clock output of 48 bit/Slot (2.1168MHz), 4.2336MHz when ESP ON
15	C2PO	0	C2 Pointer for output audio data
16	VREFL2	I	Input terminal2 of reference voltage "L" (Floating)
17	VREFL1	I	Input terminal1 of reference voltage "L" (GND connection)
18	AVDD2	-	Analog VCC2
19	RCHOUT	0	Right-Channel audio output through D/A converter
20	LCHOUT	0	Left-Channel audio output through D/A converter
21	AVSS2	-	Analog ground2
22	VREFH1	I	Input terminal1 of reference voltage "H" (VDD connection)
23	VREFH2	ı	Input terminal2 of reference voltage "H" (Floating)
24	EMPH	0	Emphasis/Non-Emphasis output, H:Emphasis ON, L:Emphasis OFF
25	LKFS	0	The Lock Status output of frame sync
26	S0S1	0	Output of subcode sync signal (S0+S1)
27	RESET	I	System reset at "L"
28	/ESP	I	ESP function ON/OFF control ("L":ESP function ON, "H":ESP function OFF)
29	SQCK	I	Clock for output Subcode-Q data
30	SQDT	0	Serial output of Subcode-Q data
31	SQOK	0	The CRC (Cycle Redundancy Check) check result signal output of Subcode-Q
32	SBCK	ı	Clock for output subcode data
33	SDAT	0	Subcode serial data output
34	DVDD1	-	Digital VDD1
35	MUTE	I	Mute control input ("H": Mute ON)

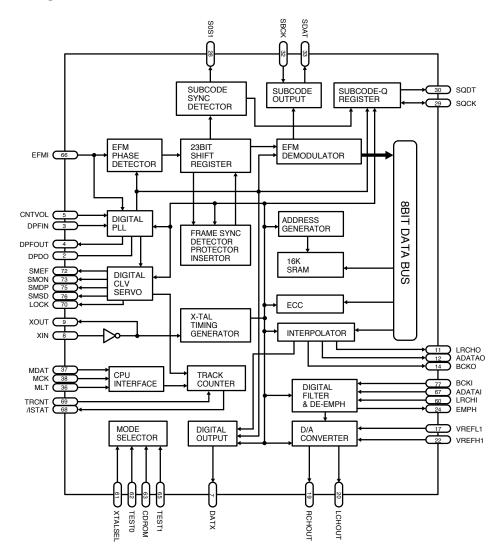
PIN DESCRIPTION (continued)

PIN NO	SYMBOL	Ю	DESCRIPTION
36	MLT	I	Latch Signal Input from Micom (Schmit Trigger)
37	MDAT	I	Serial data input from Micom (Schmit Trigger)
38	MCK	I	Serial clock input from Micom (Schmit Trigger)
39	DB8	I/O	SRAM data I/O port 8 (MSB)
40	DB7	I/O	SRAM data I/O port 7
41	DB6	I/O	SRAM data I/O port 6
42	DB5	I/O	SRAM data I/O port 5
43	DB4	I/O	SRAM data I/O port 4
44	DB3	I/O	SRAM data I/O port 3
45	DB2	I/O	SRAM data I/O port 2
46	DB1	I/O	SRAM data I/O port 1 (LSB)
47	C1F1	I/O	Monitoring output for C1 error correction (RA1)
48	C1F2	I/O	Monitoring output for C1 error correction (RA2)
49	C2F1	I/O	Monitoring output for C2 error correction (RA3)
50	C2F2	I/O	Monitoring output for C2 error correction (RA4)
51	C2FL1	I/O	C2 decoder flag (RA5, "H":When the processing C2 code is impossible correction status.)
52	/PBCK	I/O	Output of VCO/2 (4.3218MHz) (RA6)
53	DVSS2	I/O	Digital ground 2
54	FSDW	I/O	Window or unprotected frame sync (RA7)
55	ULKFS	I/O	Frame sync protection state (RA8)
56	/JIT	I/O	Display of either RAM overflow or underflow for ±4 frame jitter margin (RA9)
57	C4M	I/O	Only monitoring signal (4.2336MHz) (RA10)
58	C16M	I/O	16.9344MHz signal output (RA11)
59	/WE	I/O	Terminal for test
60	/CS	I/O	Terminal for test
61	XTALSEL	I	Mode Selection 1 (H: 33.8688MHz, L: 16.9344MHz)
62	TEST0	I	TEST input terminal (GND connection)
63	CDROM	I	Mode Selection2 (H: CDROM, L: CDP)
64	SRAM	I	TEST input terminal (GND connection)
65	TEST1	I	TEST input terminal (GND connection)
66	EFMI	I	EFM signal input
67	ADATAI	I	Serial audio data input of 48 bit/Slot (MSB first)
68	/ISTAT	0	The internal status output
69	TRCNT	I	Tracking counter input signal

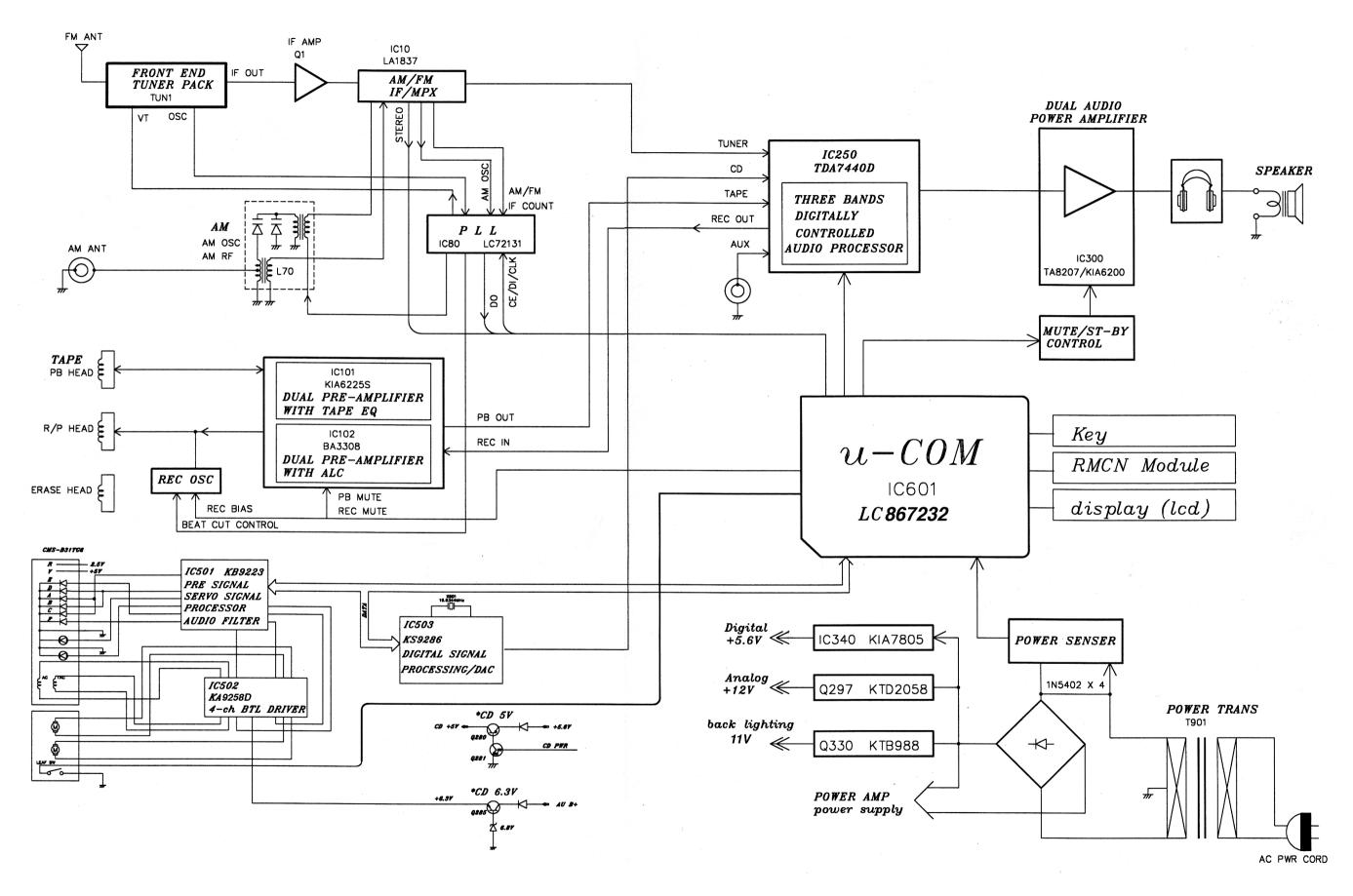
PIN DESCRIPTION (continued)

PIN NO	SYMBOL	Ю	DESCRIPTION
70	LOCK	0	Output signal of LKFS condition sampled PBFR/16 (if LKFS is "H", LOCK is "H", if LKFS is sampled "L" at least 8 times by PBFR/16, LOCK is "L".)
71	PBFR	0	Write frame clock (Lock: 7.35KHz)
72	SMEF	0	LPF time constant control of the spindle servo error signal
73	SMON	0	ON/OFF control signal for spindle servo
74	DVDD2	-	Digital VDD2
75	SMDP	0	Spindle Motor drive (Rough control in the SPEED mode, Phase control in the PHASE mode)
76	SMSD	0	Spindle Motor drive (Velocity control in the PHASE mode)
77	BCKI	I	Audio data bit clock input of 48 bit/Slot (2.1168MHz)
78	TESTV	ı	TEST input terminal (GND connection)
79	DSPEED	I	TEST input terminal (VDD connection)
80	LRCHI	I	Channel clock input of 48 bit/Slot (44.1KHz)

BLOCK DIAGRAM

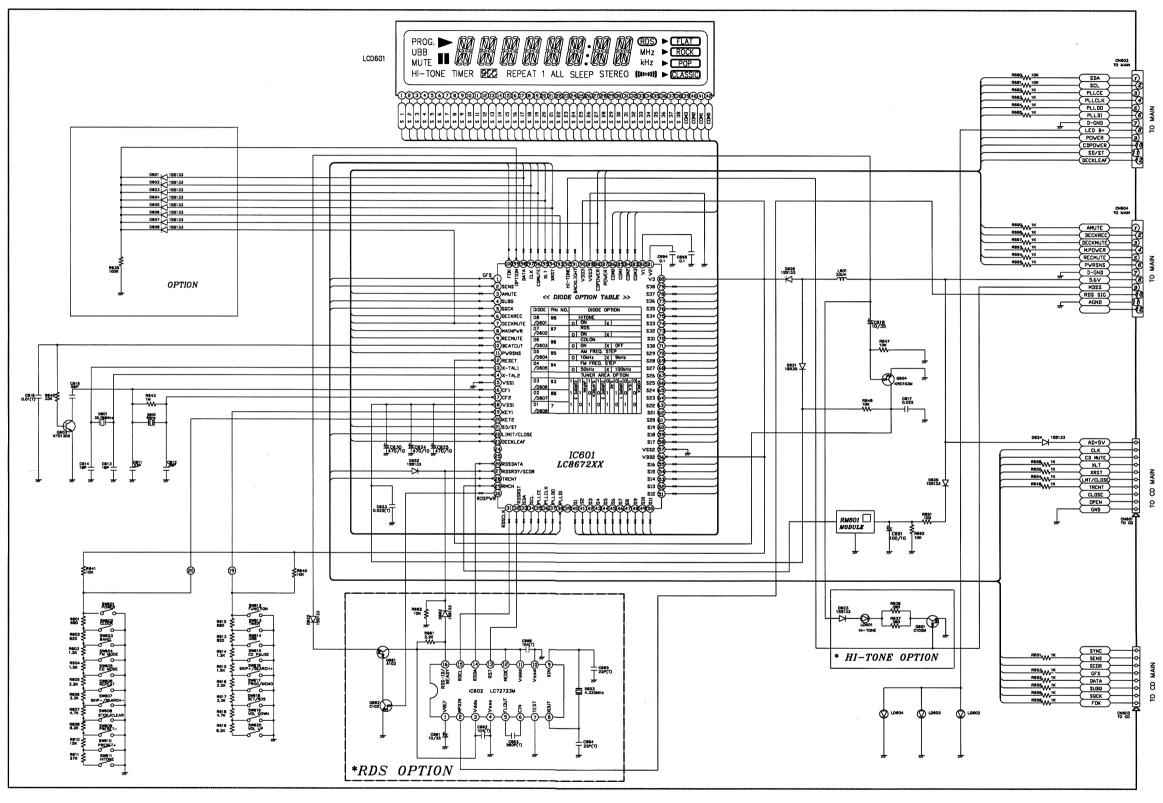


BLOCK DIAGRAM



SCHEMATIC DIAGRAMS

FRONT & KEY CIRCUIT



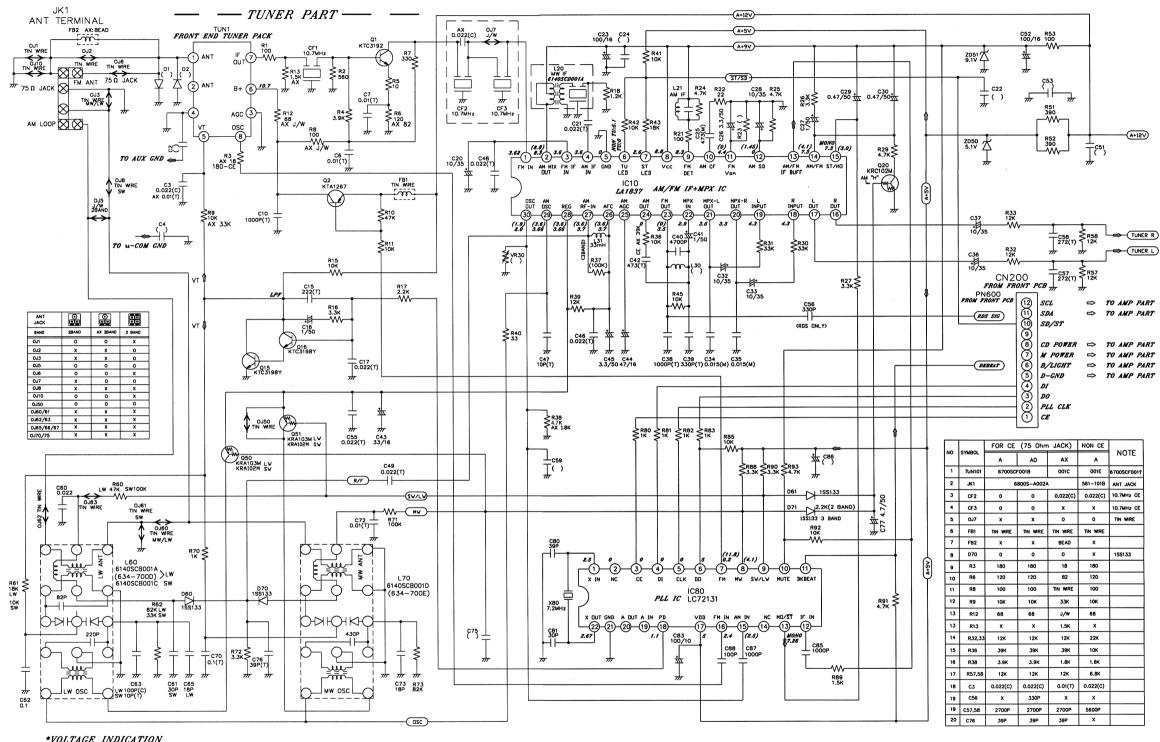
RC102M OC KRC103M OC KRA102M OC BO-MI BO-M

NOTES: 1. Resistance values are indicted in ohms unless otherwise specified (K=1,000, M=1,000,000).

2. Capacitance values are shown in microfarads unless otherwise (P=MICRO-MICRO FARADS).

3. Schematic diagram for this model are subject to change for improvement without prior notice.

TUNER CIRCUIT



*VOLTAGE INDICATION
1.FM 2.()AM

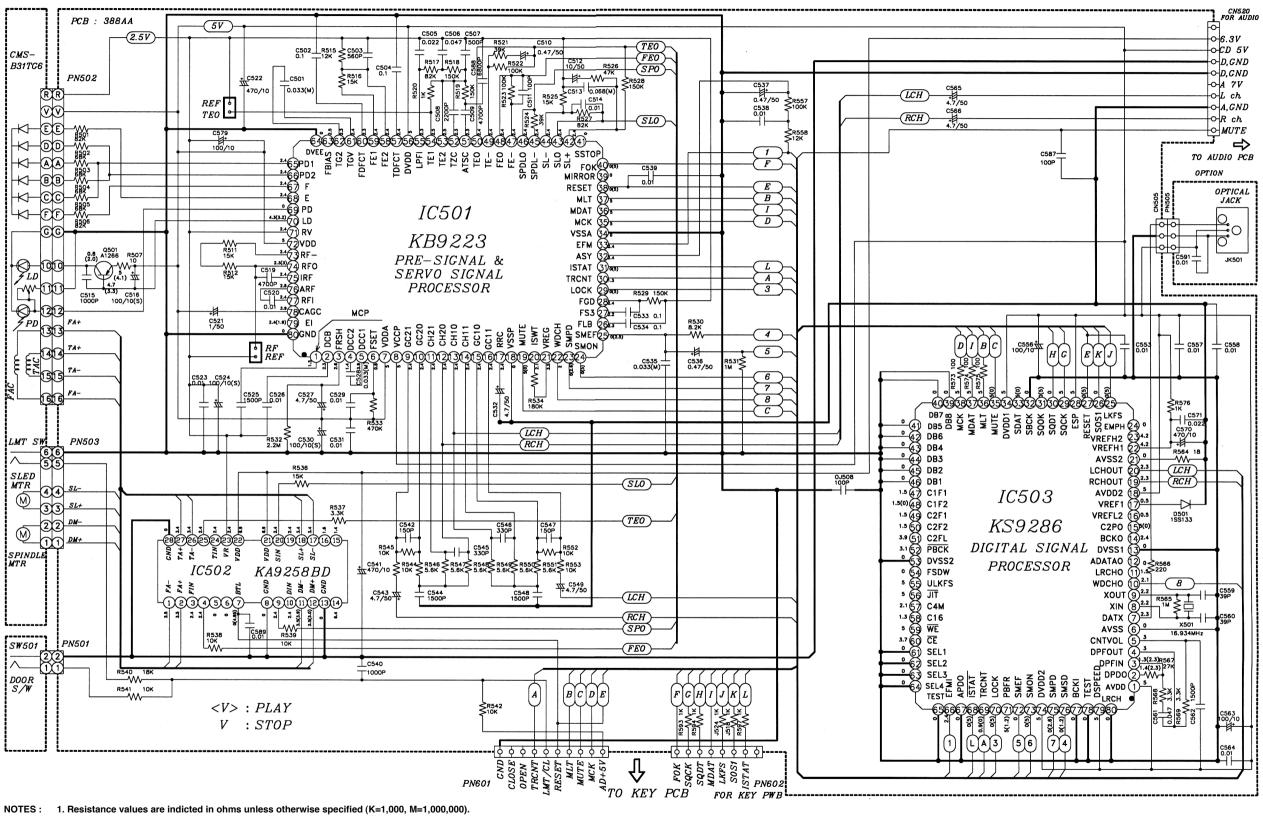
NOT USED: D1,D2 L30
VR30 R23
C2,22,24,43,51,53,59

NOTES: 1. Resistance values are indicted in ohms unless otherwise specified (K=1,000, M=1,000,000).

2. Capacitance values are shown in microfarads unless otherwise (P=MICRO-MICRO FARADS).

3. Schematic diagram for this model are subject to change for improvement without prior notice.

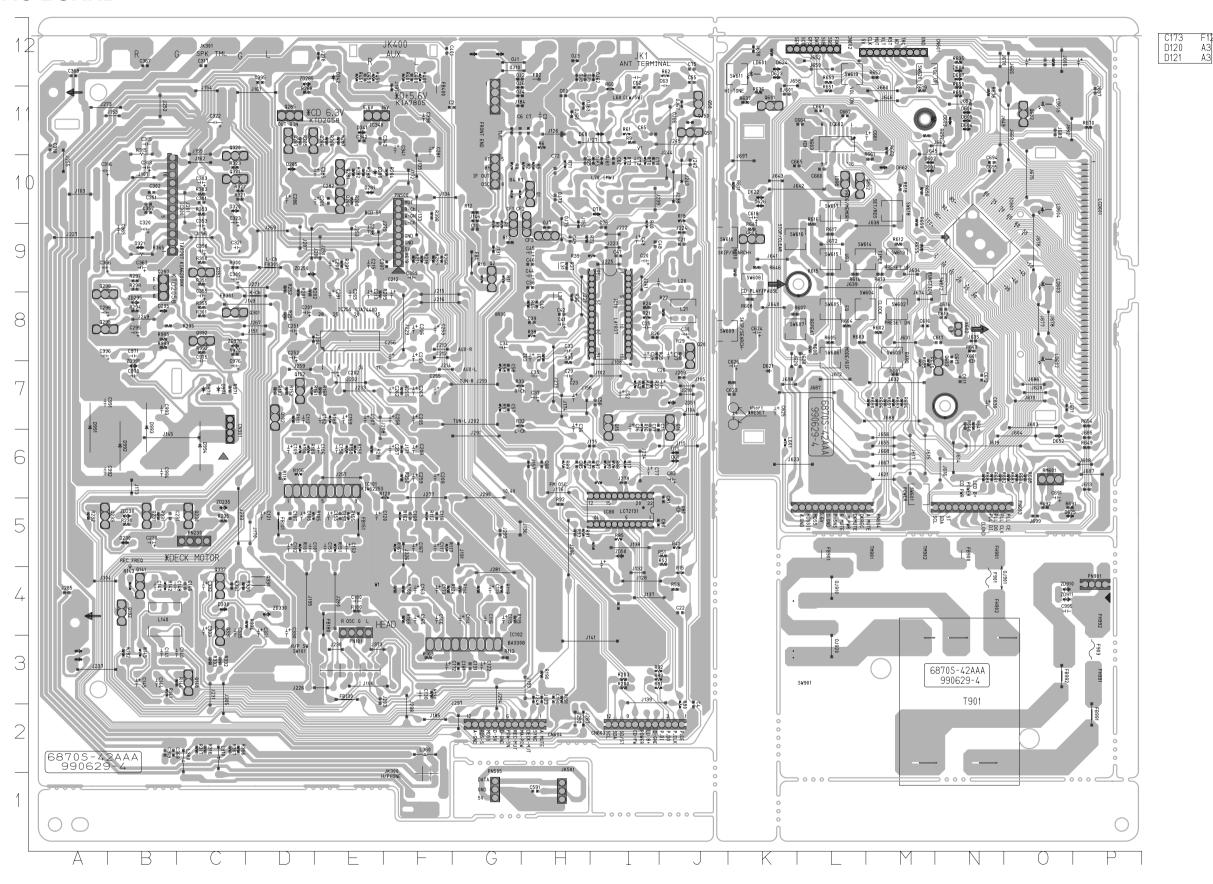
CDP CIRCUIT



- NOTES: 1. Resistance values are indicted in ohms unless otherwise specified (K=1,000, M=1,000,000).
 - 2. Capacitance values are shown in microfarads unless otherwise (P=MICRO-MICRO FARADS).
 - 3. Schematic diagram for this model are subject to change for improvement without prior notice.

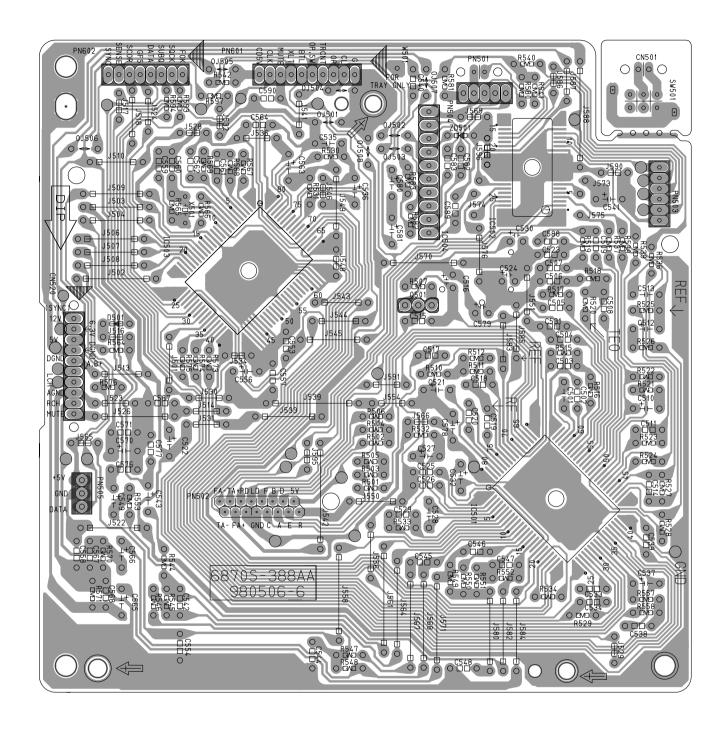
PCB LAYOUTS

• MAIN P.C BOARD

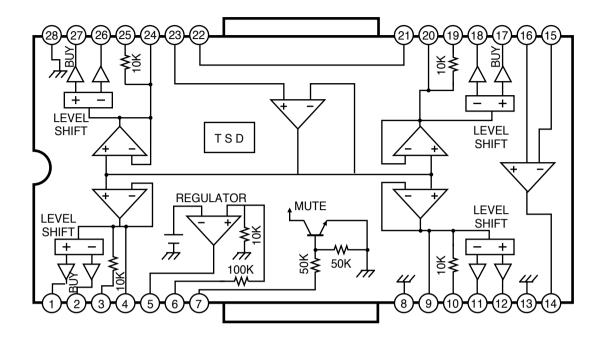


INTERNAL BLOCK DIAGRAM OF ICs

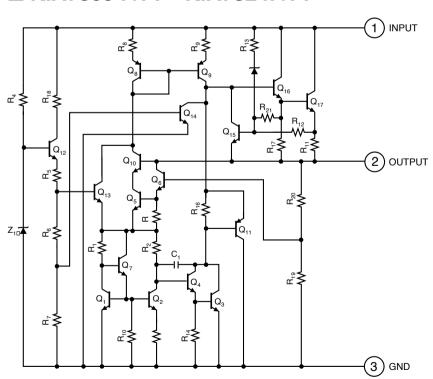
• CDP P.C BOARD



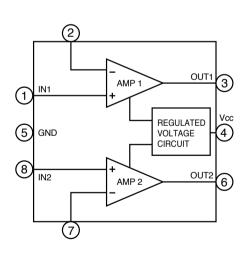
■ KA3010D



■ KIA7805 P/PI ~ KIA7824P/PI



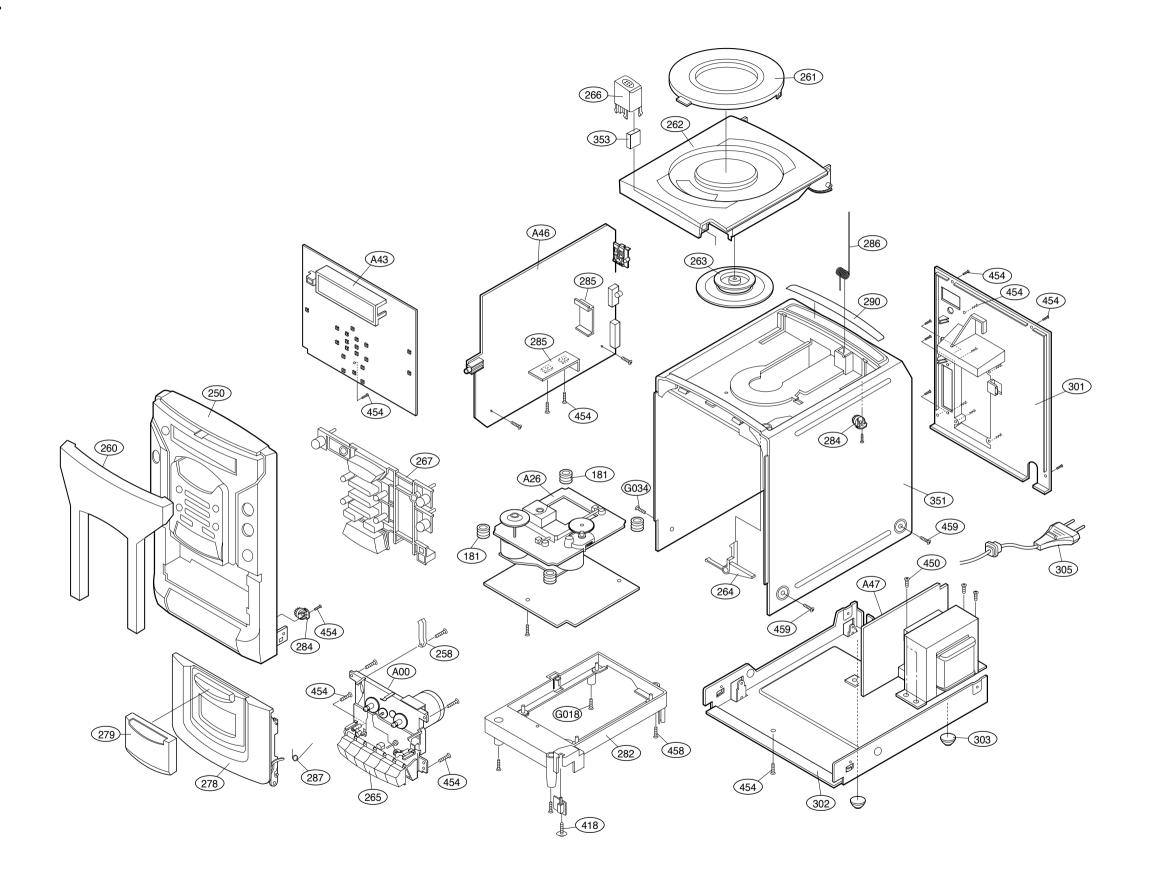
■ KIA6225S



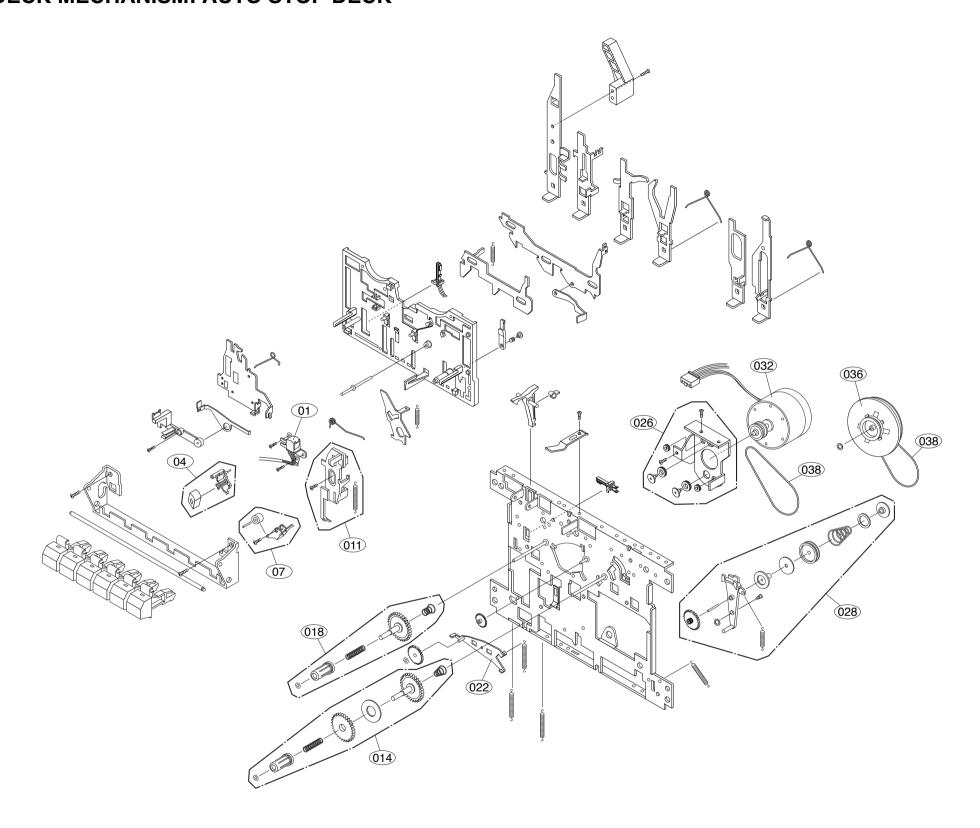
- 26 -

EXPLODED VIEW/PARTS LIST

CABINET

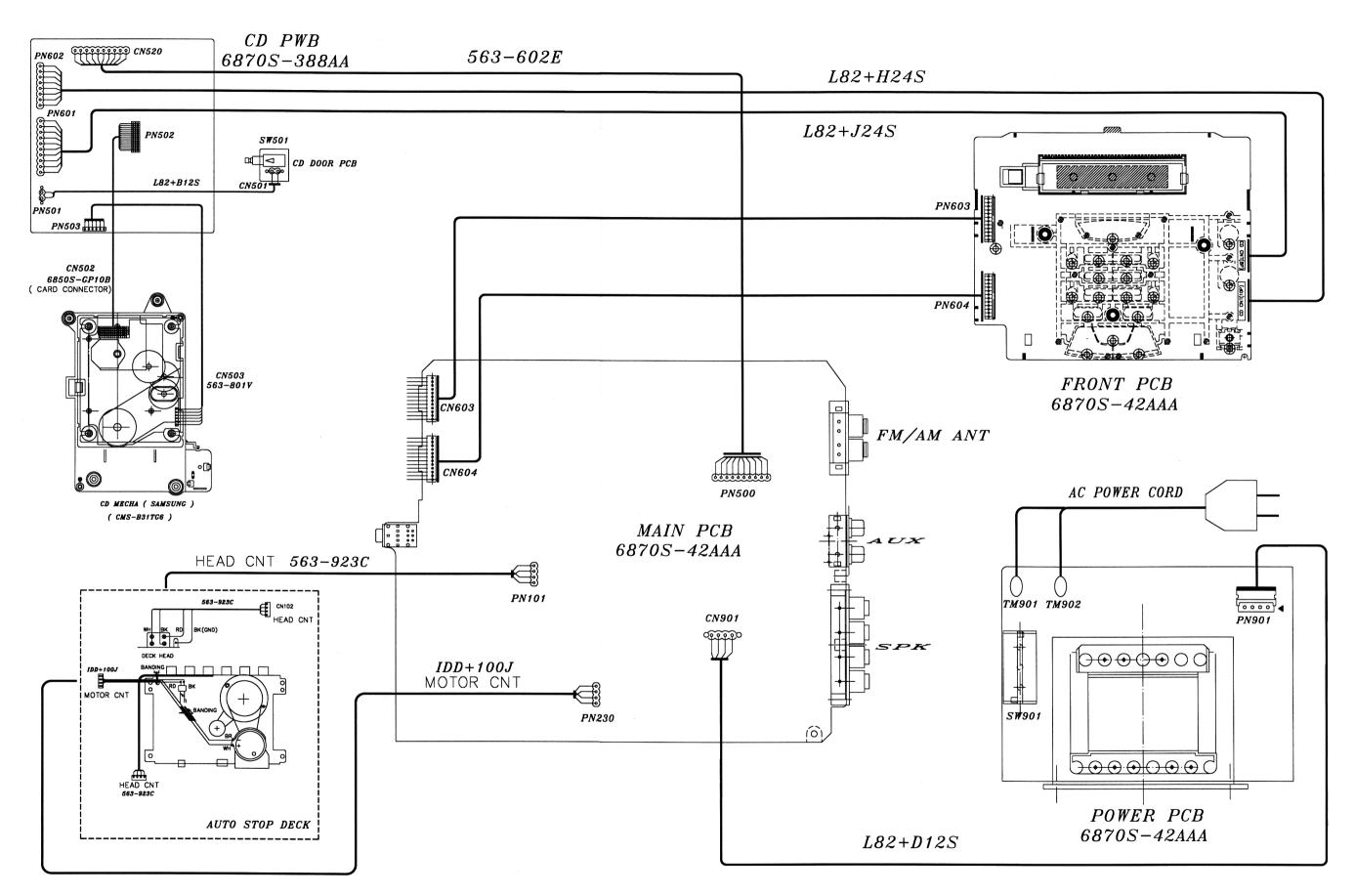


• TAPE DECK MECHANISM: AUTO STOP DECK



- 39 -

WIRING DIAGRAM



NOTE: Warning

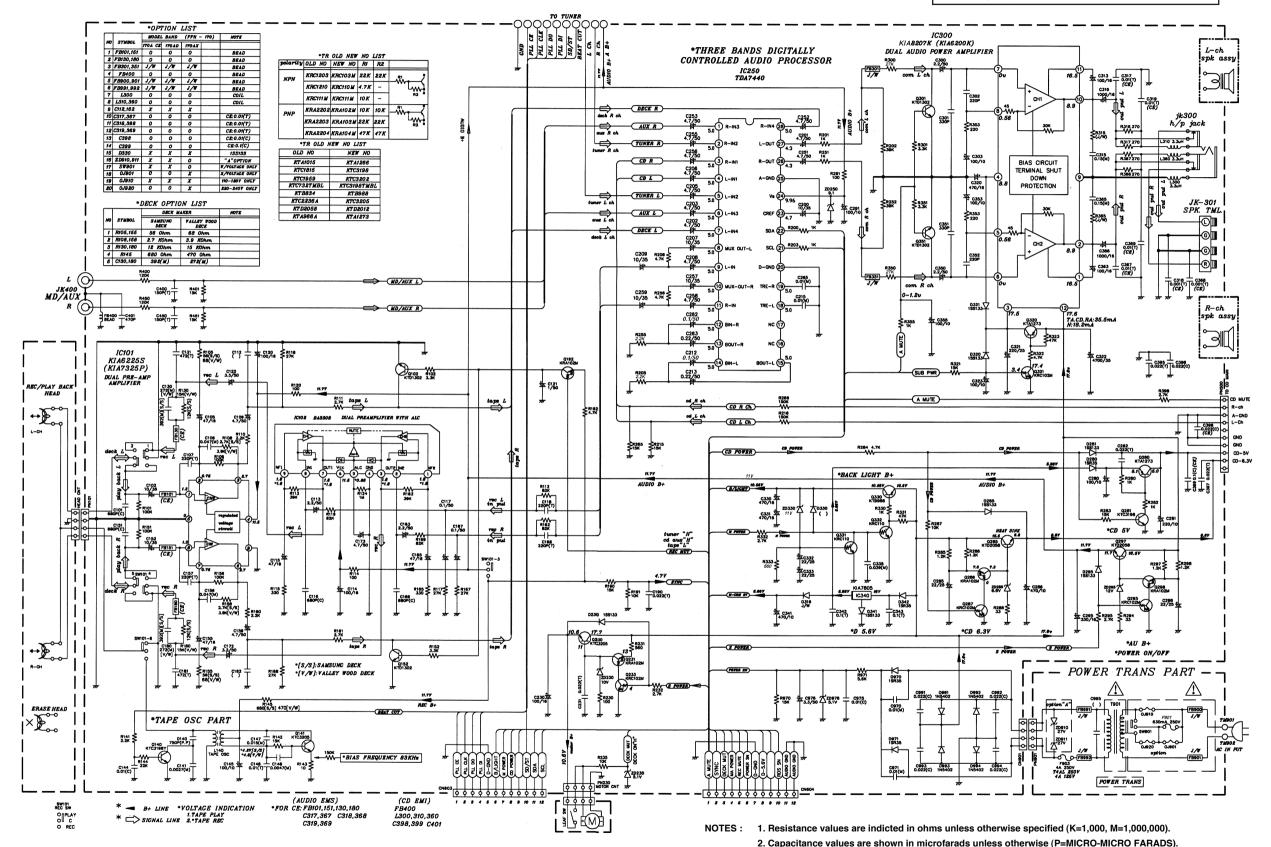
AMP & DECK CIRCUIT

Parts that are shaded are critical With respect to risk of fire or electrical shock.

NOTE:

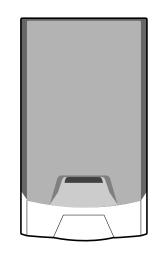
3. Schematic diagram for this model are subject to change for improvement without prior notice.

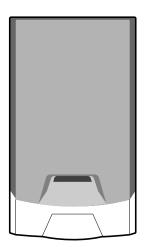
- Voltages are DC-measured with a digital voltmefer during Play mode.



SPEAKER SYSTEM

MODEL: FE-175E





SPECIFICATION

• TYPE : BASS REFLEX 1 WAY 1 SPEAKER SYSTEM

SPEAKER SYSTEM : WOOTER 100mm(4")
 FREQUENCY RESPONSE : 90Hz~20.000Hz

• IMPEDANCE : 4Ω

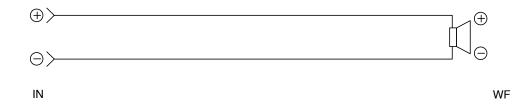
• S.P.L. : 86dB/W(1m)

RATED INPUT POWER : 5WMAX. INPUT POWER : 10W

• DIMENSION NET : 148(W) x 240(H) x 183(D)mm

• WEIGHT NET : 1.52kg

SCHEMATIC DIAGRAM



EXPLODED VIEW/PARTS LIST

